# MSC8103

## Network Digital Signal Processor
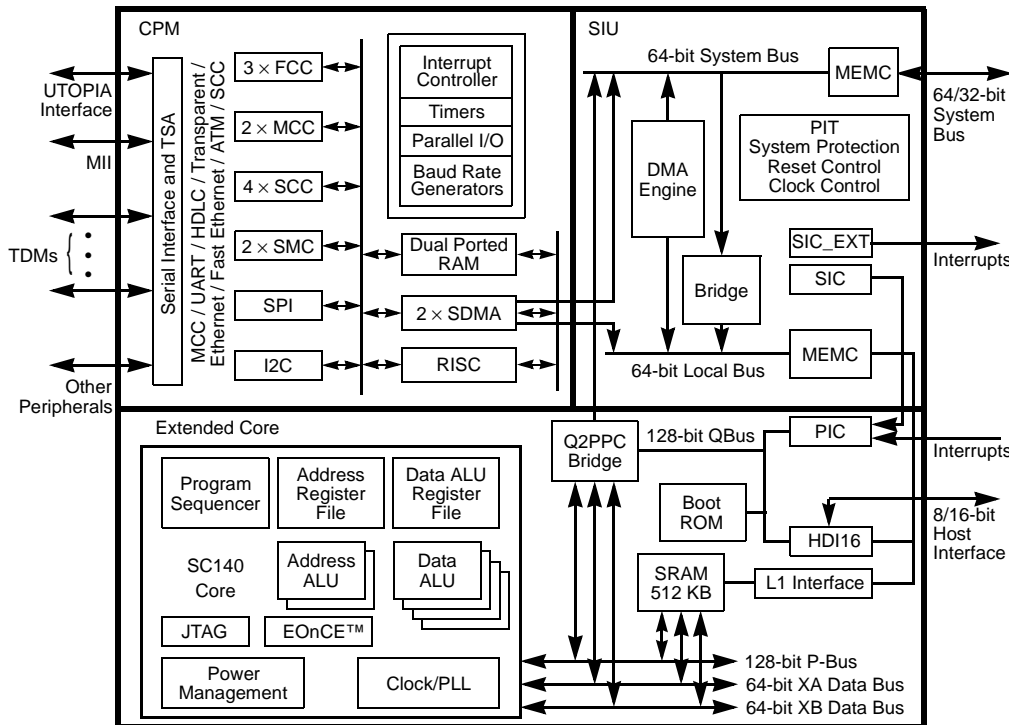


*The Freescale MSC8103 16-bit DSP is a member of the family of DSPs based on the StarCore SC140 DSP core. The MSC8103 is available in two core speed levels: 275 and 300 MHz.*

**What's New?**
Rev. 12 includes the following changes:
- **Table 2-4** changes $V_{IL}$ reference for signal low input current to 0.8 V.

**Figure 1.** MSC8103 Block Diagram

The Freescale MSC8103 DSP is a very versatile device that integrates the high-performance SC140 four-ALU (arithmetic logic unit) DSP core along with 512 KB of internal memory, a communications processor module (CPM), a 64-bit bus, a very flexible system integration unit (SIU), and a 16-channel DMA engine on a single device. With its four-ALU core, the MSC8103 can execute up to four multiply-accumulate (MAC) operations in a single clock cycle. The MSC8103 CPM is a 32-bit RISC-based communications protocol engine that can network to time-division multiplexed (TDM) highways, Ethernet, and asynchronous transfer mode (ATM) backbones. The MSC8103 60x-compatible bus interface facilitates its connection to multi-master system architectures. The very large internal memory, 512 KB, reduces the need for external program and data memories. The MSC8103 offers 1200 DSP MMACS performance using an internal 300 MHz clock with a 1.6 V core and independent 3.3 V input/output (I/O).

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# Data Sheet Conventions

| | |
|---|---|
| pin and pin-out | Although the device package does not have pins, the term pins and pin-out are used for convenience and indicate specific signal locations within the ball-grid array. |
| $\overline{\text{OVERBAR}}$ | Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.) |
| "asserted" | Means that a high true (active high) signal is high or that a low true (active low) signal is low |
| "deasserted" | Means that a high true (active high) signal is low or that a low true (active low) signal is high |

Examples:

| Signal/Symbol | Logic State | Signal State | Voltage |
|---|---|---|---|
| $\overline{\text{PIN}}$ | True | Asserted | $V_{IL}/V_{OL}$ |
| $\overline{\text{PIN}}$ | False | Deasserted | $V_{IH}/V_{OH}$ |
| PIN | True | Asserted | $V_{IH}/V_{OH}$ |
| PIN | False | Deasserted | $V_{IL}/V_{OL}$ |

**Note:**   Values for $V_{IL}$, $V_{OL}$, $V_{IH}$, and $V_{OH}$ are defined by individual product specifications.

# MSC8103 Features

- SC140 core
  - Architecture optimized for efficient C/C++ code compilation
  - Four 16-bit ALUs and two 32-bit AGUs
  - 1200 DSP MMACS running at 300 MHz
  - Very low power dissipation
  - Variable-length execution set (VLES) execution model
  - JTAG/Enhanced OnCE debug port
- Communications processor module (CPM)
  - Programmable protocol machine using a 32-bit RISC engine
  - 155 Mbps ATM interface (including AAL 0/1/2/5)
  - 10/100 Mbit Ethernet interface
  - Up to four E1/T1 interfaces or one E3/T3 interface and one E1/T1 interface
  - HDLC support up to T3 rates, or 256 channels
- 64- or 32-bit wide bus interface
  - Support for bursts for high efficiency
  - Glueless interface to 60x-compatible bus systems
  - Multi-master support
- Programmable memory controller
  - Control for up to eight banks of external memory
  - User-programmable machines (UPM) allowing glueless interface to various memory types (SRAM, DRAM, EPROM, and Flash memory) and other user-definable peripherals
  - Dedicated pipelined SDRAM memory interface
- Large internal SRAM
  - 256K 16-bit words (512 KB)
  - Unified program and data space configurable by the application
  - Word and byte addressable
- DMA controller
  - 16 DMA channels, FIFO based, with burst capabilities
  - Sophisticated addressing capabilities
- Small foot print package
  - 17 mm × 17 mm lidded FC-PBGA package with lead-bearing or lead-free spheres
- Very low power consumption
  - Separate power supply for internal logic (1.6 V) and for I/O (3.3 V)
- Enhanced 16-bit parallel host interface (HDI16)
  - Supports a variety of microcontroller, microprocessor, and DSP bus interfaces
- Phase-lock loops (PLLs)
  - System PLL
  - CPM DPLLs (SCC and SCM)
- Process technology
  - 0.13 micron copper interconnect process technology

# Target Applications

The MSC8103 targets applications requiring very high performance, very large amounts of internal memory, and such networking capabilities as:

- Third-generation wideband wireless infrastructure systems
- Packet Telephony systems
- Multi-channel modem banks
- Multi-channel xDSL

# Product Documentation

The documents listed in **Table 1** are required for a complete description of the MSC8103 and are necessary to design properly with the part. Documentation is available from the following sources (see back cover for details):

- A local Freescale distributor
- A Freescale Semiconductor sales office
- A Freescale Semiconductor Literature Distribution Center
- The world wide web (WWW)

**Table 1.** MSC8103 Documentation

| Name | Description | Order Number |
|---|---|---|
| MSC8103 Technical Data | MSC8103 features list and physical, electrical, timing, and package specifications | MSC8103/D |
| MSC8101 User's Guide | Detailed functional description of the MSC8101 memory configuration, operation, and register programming. All details apply to the MSC8103. | MSC8101UG/D |
| MSC8103 Reference Manual | Detailed description of the MSC8103 processor core and instruction set | MSC8103RM/D |
| SC140 DSP Core Reference Manual | Detailed description of the SC140 family processor core and instruction set | MNSC140CORE/D |
| Application Notes | Documents describing specific applications or optimized device operation including code examples | See the MSC8103 product website |

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# Signals/Connections 1

The MSC8103 external signals are organized into functional groups, as shown in **Table 1-1**, **Figure 1-1**, and **Figure 1-2**. **Table 1-1** lists the functional groups, states the number of signal connections in each group, and references the table that gives details on multiplexed signals within each group. **Figure 1-1** shows MSC8103 external signals organized by function. **Figure 1-2** indicates how the parallel input/output (I/O) ports signals are multiplexed. Because the parallel I/O design supported by the MSC8103 communications processor module (CPM) is a subset of the parallel I/O signals supported by the MPC8260 device, port pins are not numbered sequentially.

**Table 1-1.** MSC8103 Functional Signal Groupings

| Functional Group | | Number of Signal Connections | Detailed Description |
|---|---|---|---|
| Power (V$_{CC}$, V$_{DD}$, and GND) | | 80 | **Table 1-2** on page 1-4 |
| Clock | | 6 | **Table 1-3** on page 1-4 |
| Reset, configuration, and EOnCE | | 11 | **Table 1-4** on page 1-5 |
| System bus, HDI16, and interrupts | | 133 | **Table 1-5** on page 1-7 |
| Memory controller | | 27 | **Table 1-6** on page 1-13 |
| CPM input/output parallel ports | Port A | 26 | **Table 1-7** on page 1-16 |
| | Port B | 14 | **Table 1-8** on page 1-21 |
| | Port C | 18 | **Table 1-9** on page 1-24 |
| | Port D | 8 | **Table 1-10** on page 1-33 |
| JTAG test access port (TAP) | | 5 | **Table 1-11** on page 1-36 |
| Reserved (denotes connections that are always reserved) | | 5 | **Table 1-12** on page 1-36 |

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VDD → 14
VDDH → 25
VCCSYN → 1
VCCSYN1 → 1

POWER

GND → 37
GNDSYN → 1
GNDSYN1 → 1

32 ↔ **A[0–31]**
5 ↔ **TT[0–4]**
4 ↔ **TSIZ[0–3]**
1 ↔ **TBST**
1 ↔ **IRQ1**          GBL
3 → **Reserved**      BADDR[29–31]                    IRQ[2–3, 5]
1 ↔ **BR**
1 ↔ **BG**
1 ↔ **ABB**          IRQ2
1 ↔ **TS**
1 ↔ **AACK**
1 ← **ARTRY**
1 ↔ **DBG**
1 ↔ **DBB**          IRQ3
32 ↔ **D[0–31]**

CPM I/O PORTS

Port A
PA[31–6] ↔ 26

Port B
PB[31–18] ↔ 14

For the signals multiplexed on Ports A–D, see **Figure 1-2**

Port C
PC[31–22, 15–12, 7–4] ↔ 18

Port D
PD[31–29, 19–16, 7] ↔ 8

60x BUS

16 ↔ **D[32–47]**
4 ↔ **D[48–51]**
1 ↔ **D52**
1 ↔ **D53**
1 ↔ **D54**
1 ↔ **D55**
1 ↔ **D56**
1 ↔ **D57**
1 ↔ **D58**
1 ↔ **D59**
1 ↔ **D60**
4 ↔ **D[61–63]**

| HDI16 Signals | | |
|---|---|---|
| HD[0–15] | | |
| HA[0–3] | | |
| HCS1 | | |
| *Single DS* | | *Double DS* |
| HRW | | HRD/HRD |
| HDS/HDS | | HWR/HWR |
| *Single HR* | | *Double HR* |
| HREQ/HREQ | | HTRQ/HTRQ |
| HACK/HACK | | HRRQ/HRRQ |
| HDSP | | |
| HDDS | | |
| H8BIT | | |
| HCS2 | | |
| Reserved | | |

TMS → 1
TDI → 1
TCK → 1
TRST → 1
TDO ← 1

JTAG

EOnCE Event
EED ↔ 1
EE0
EE1
EE[2–3] ↔ 2
EE[4–5]

RESET Configuration
DBREQ ↔ 1
HPE ↔ 1

BTM[0–1] ↔ 2
PORESET → 1
RSTCONF → 1
HRESET ↔ 1
SRESET ↔ 1

1 ← **Reserved**    DP0    Reserved    EXT_Br2
1 ↔ **IRQ1**        DP1    IRQ1        EXT_BG2
1 ↔ **IRQ2**        DP2    Reserved    EXT_DBG2
1 ↔ **IRQ3**        DP3    Reserved    EXT_BR3
1 ↔ **IRQ4**        DP4    DREQ3       EXT_BG3
1 ↔ **IRQ5**        DP5    DREQ4       EXT_DBG3
1 ↔ **IRQ6**        DP6    DACK3       IRQ6
1 ↔ **IRQ7**        DP7    DACK4       IRQ7
1 ↔ **TA**
1 ↔ **TEA**
1 ← **NMI**
1 → **NMI_OUT**
1 ↔ **PSDVAL**
1 ↔ **IRQ7**        INT_OUT

BNK-SEL[0–2]    TC[0–2]

CLKIN → 1
MODCK[1–3] → 3
CLKOUT ← 1
DLLIN → 1

MEMC

8 → **CS[0–7]**
1 → **BCTL1**
2 → **BADDR[27–28]**
1 → **ALE**
1 → **BCTL0**
8 → **PWE[0–7]**    PSDDQM[0–7]              PBS[0–7]
1 → **PSDA10**                              PGPL0
1 → **PSDWE**                               PGPL1
1 → **POE**                      PSDRAS     PGPL2

TEST → 1
THERM[1–2] ↔ 2
SPARE1, SPARE5 ↔ 2

1 → **PSDCAS**                              PGPL3
1 ↔ **PGTA**        PUPMWAIT     PPBS       PGPL4
1 → **PSDAMUX**                             PGPL5

**Note:** Refer to the *System Interface Unit (SIU)* chapter in the *MSC8103 Reference Manual* for details on how to configure these pins.

**Figure 1-1.** MSC8103 External Signals

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**Figure 1-2.** CPM Port A–D Pin Multiplexed Functionality

Port A (PA31–PA6):

| FCC1 ATM/UTOPIA (MPHY Master mux poll or Slave) | FCC1 ATM (MPHY Master dir. poll) | FCC1 Ethernet MII | FCC1 HDLC/transp. Serial | FCC1 HDLC Nibble | SI1 TDMA1 Serial | SI1 TDMA1 Nibble | SMC2 | SDMA | GPIO |
|---|---|---|---|---|---|---|---|---|---|
| TXENB | | COL | | | | | | | PA31 |
| TXCLAV | TXCLAV0 | CRS | RTS | | | | | | PA30 |
| TXSOC (master) | | TX_ER | | | | | | | PA29 |
| RXENB | | TX_EN | | | | | | | PA28 |
| RXSOC (slave) | | RX_DV | | | | | | | PA27 |
| RXCLAV | RXCLAV0 | RX_ER | | | | | | SDMA | PA26 |
| TXD0 | | | | | | | | MSNUM0 | PA25 |
| TXD1 | | | | | | | | MSNUM1 | PA24 |
| TXD2 | | | | | | | | | PA23 |
| TXD3 | | | | | | | | | PA22 |
| TXD4 | | TXD3 | | TXD3 | | | | | PA21 |
| TXD5 | | TXD2 | | TXD2 | | | | | PA20 |
| TXD6 | | TXD1 | | TXD1 | | | | | PA19 |
| TXD7 | | TXD0 | TXD | TXD0 | | | | | PA18 |
| RXD7 | | RXD0 | RXD | RXD0 | | | | | PA17 |
| RXD6 | | RXD1 | | RXD1 | | | | | PA16 |
| RXD5 | | RXD2 | | RXD2 | | | | | PA15 |
| RXD4 | | RXD3 | | RXD3 | | | | | PA14 |
| RXD3 | | | | | | | | MSNUM2 | PA13 |
| RXD2 | | | | | | | | MSNUM3 | PA12 |
| RXD1 | | | | | | | | MSNUM4 | PA11 |
| RXD0 | | | | | | | | MSNUM5 | PA10 |
| | | | | | | | | | PA9 |
| | | | | | | | SMTXD / L1TXD / L1TXD0 | | PA9 |
| | | | | | | | SMRXD / L1RXD / L1RXD0 | | PA8 |
| | | | | | | | SMSYN / L1TSYNC | | PA7 |
| | | | | | | | L1RSYNC | SI2 | PA6 |

Port B (PB31–PB18):

| FCC2 Ethernet MII | FCC2 HDLC/transp. Serial | FCC2 HDLC Nibble | SCC2 | SI1 | SI2 | I2C | GPIO |
|---|---|---|---|---|---|---|---|
| TX_ER | | | RXD | | TDMB2 L1TXD | | PB31 |
| RX_DV | | | TXD | | L1RXD | | PB30 |
| TX_EN | | | | | L1RSYNC | | PB29 |
| RX_ER | RTS | | RTS/TENA | | L1TSYNC | | PB28 |
| COL | | | | | TDMC2 L1TXD | | PB27 |
| CRS | | | | | L1RXD | | PB26 |
| TXD3 | | TXD3 | | L1TXD3 | L1TSYNC | | PB25 |
| TXD2 | | TXD2 | | L1RXD3 | L1RSYNC | | PB24 |
| TXD1 | | TXD1 | | L1RXD2 | TDMD2 L1TXD | | PB23 |
| TXD0 | TXD | TXD0 | | L1RXD1 | L1RXD | | PB22 |
| RXD0 | RXD | RXD0 | | L1TXD2 | L1TSYNC | | PB21 |
| RXD1 | | RXD1 | | L1TXD1 | L1RSYNC | I2C | PB20 |
| RXD2 | | RXD2 | | | | SDA | PB19 |
| RXD3 | | RXD3 | | | | SCL | PB18 |

Port C (PC31–PC4):

| FCC1 ATM | FCC1 ATM | SCC / Ext. Req. | SCC2 | SMC2 | SI1 LIST | DMA / SIU Timer Input | BRGs | Clocks | Timers | GPIO |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Ext. Req. EXT1 | | | | | BRG1O | CLK1 | TGATE1 | PC31 |
| | | | | | | | BRG2O | CLK2 | TOUT1 | PC30 |
| | | SCC1 CTS/CLSN | | | | | BRG3O | CLK3 | TIN2 | PC29 |
| | | | CTS/CLSN | | | SIU Timer Input | BRG4O | CLK4 | TIN1/TOUT2 | PC28 |
| | | | | | | CLK5 | BRG5O | CLK5 | TGATE2 | PC27 |
| | | | | | | TMCLK | BRG6O | CLK6 | TOUT3 | PC26 |
| | | | | | | DMA DACK2 | BRG7O | CLK7 | TIN4 | PC25 |
| | | | | | | DREQ2 | BRG8O | CLK8 | TIN3/TOUT4 | PC24 |
| | | | | | | DACK1 | | CLK9 | | PC23 |
| | | Ext. Req. EXT2 | | | LIST1 | DREQ1 | | CLK10 | | PC22 |
| TXADDR0 | | SCC1 CTS/CLSN | | SMTXD | | | | | | PC15 |
| RXADDR0 | | CD/RENA | | | LIST2 | | | | | PC14 |
| TXADDR1 | | | | | LIST4 | | | | | PC13 |
| RXADDR1 | | | CTS/CLSN | CD/RENA | LIST3 | | | | | PC12 |
| TXADDR2 | TXADDR2/TXCLAV1 | FCC1 CTS | | | LIST1 | | | | | PC7 |
| RXADDR2 | RXADDR2/RXCLAV1 | FCC1 CD | | | LIST2 | | | | | PC6 |
| | | FCC2 CTS | | SMC1 SMTXD | LIST3 | | | | | PC5 |
| | | FCC2 CD | | SMC1 SMRXD | LIST4 | | | | | PC4 |

Port D (PD31–PD7):

| FCC1 ATM | FCC1 ATM | SCC2 | SMC1 | DMA | SPI | BRG | GPIO |
|---|---|---|---|---|---|---|---|
| | | RXD | | DRACK1/DONE1 | | | PD31 |
| | | TXD | | DRACK2/DONE2 | | | PD30 |
| | | RTS/TENA | | | SPI | | PD29 |
| RXADDR3 | RXCLAV2 | | | | SPISEL | BRG1O | PD19 |
| TXADDR4 | TXCLAV3 | | | | SPICLK | | PD18 |
| RXADDR4 | RXCLAV3 | | | | SPIMOSI | BRG2O | PD17 |
| RXPRTY | | | | | SPIMISO | | PD16 |
| TXADDR3 | TXCLAV2 | | SMSYN | | | | PD7 |
| TXPRTY | | | | | | | |

# 1.1  Power Signals

**Table 1-2.**   Power and Ground Signal Inputs

| Power Name | Description |
|---|---|
| $V_{DD}$ | **Internal Logic Power**<br>$V_{DD}$ dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the $V_{DD}$ power rail. |
| $V_{DDH}$ | **Input/Output Power**<br>This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors. |
| $V_{CCSYN}$ | **System PLL Power**<br>$V_{CC}$ dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the $V_{CC}$ power rail. |
| $V_{CCSYN1}$ | **SC140 PLL Power**<br>$V_{CC}$ dedicated for use with the SC140 core PLL. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the $V_{CC}$ power rail. |
| GND | **System Ground**<br>An isolated ground for the internal processing logic. This connection must be tied externally to all chip ground connections, except $GND_{SYN}$ and $GND_{SYN1}$. The user must provide adequate external decoupling capacitors. |
| $GND_{SYN}$ | **System PLL Ground**<br>Ground dedicated for system PLL use. The connection should be provided with an extremely low-impedance path to ground. |
| $GND_{SYN1}$ | **SC140 PLL Ground 1**<br>Ground dedicated for SC140 core PLL use. The connection should be provided with an extremely low-impedance path to ground. |

# 1.2  Clock Signals

**Table 1-3.**   Clock Signals

| Signal Name | Type | Signal Description |
|---|---|---|
| CLKIN | Input | **Clock In**<br>Primary clock input to the MSC8103 PLL. |
| $\overline{\text{MODCK1}}$ | Input | **Clock Mode Input 1**<br>Defines the operating mode of internal clock circuits. |
| TC0 | Output | **Transfer Code 0**<br>Supplies information that can be useful for debugging bus transactions initiated by the MSC8103. |
| BNKSEL0 | Output | **Bank Select 0**<br>Selects the SDRAM bank when the MSC8103 is in 60x-compatible bus mode. |
| $\overline{\text{MODCK2}}$ | Input | **Clock Mode Input 2**<br>Defines the operating mode of internal clock circuits. |
| TC1 | Output | **Transfer Code 1**<br>Supplies information that can be useful for debugging bus transactions initiated by the MSC8103. |
| BNKSEL1 | Output | **Bank Select 1**<br>Selects the SDRAM bank when the MSC8103 is in 60x-compatible bus mode. |
| $\overline{\text{MODCK3}}$ | Input | **Clock Mode Input 3**<br>Defines the operating mode of internal clock circuits. |
| TC2 | Output | **Transfer Code 2**<br>Supplies information that can be useful for debugging bus transactions initiated by the MSC8103. |
| BNKSEL2 | Output | **Bank Select 2**<br>Selects the SDRAM bank when the MSC8103 is in 60x-compatible bus mode. |

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**Table 1-3.** Clock Signals (Continued)

| Signal Name | Type | Signal Description |
|---|---|---|
| CLKOUT | Output | **Clock Out**<br>The system bus clock. |
| DLLIN | Input | **DLLIN**<br>Synchronizes with an external device.<br>**Note:** When the DLL is disabled, connect this signal to GND. |

# 1.3  Reset, Configuration, and EOnCE Event Signals

**Table 1-4.** Reset, Configuration, and EOnCE Event Signals

| Signal Name | Type | Signal Description |
|---|---|---|
| DBREQ | Input | **Debug Request**<br>Determines whether to go into SC140 Debug mode when $\overline{\text{PORESET}}$ is deasserted. |
| EE0[1] | | **Enhanced OnCE (EOnCE) Event 0**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EE0 as an input (default) or an output. |
| | Input | Debug request, enable Address Event Detection Channel 0, or generate an EOnCE event. |
| | Output | Detection by Address Event Detection Channel 0. Used to trigger external debugging equipment. |
| HPE | Input | **Host Port Enable**<br>When this pin is asserted during $\overline{\text{PORESET}}$, the Host port is enabled, the system data bus is 32 bits wide, and the Host *must* program the reset configuration word. |
| EE1[1] | | **EOnCE Event 1**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EE1 as an input (default) or an output. |
| | Input | Enable Address Event Detection Channel 1 or generate an EOnCE event. |
| | Output | Debug Acknowledge or detection by Address Event Detection Channel 1. Used to trigger external debugging equipment. |
| EE2[1] | | **EOnCE Event 2**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EE2 as an input (default) or an output. |
| | Input | Enable Address Event Detection Channel 2 or generate an EOnCE event or enable the Event Counter. |
| | Output | Detection by Address Event Detection Channel 2. Used to trigger external debugging equipment. |
| EE3[1] | | **EOnCE Event 3**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EE3 as an input (default) or an output. See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on the ERCV Register. |
| | Input | Enable Address Event Detection Channel 3 or generate one of the EOnCE events. |
| | Output | The DSP has read the EOnCE Receive Register (ERCV). Triggers external debugging equipment. |

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**Table 1-4.** Reset, Configuration, and EOnCE Event Signals (Continued)

| Signal Name | Type | Signal Description |
|---|---|---|
| BTM[0–1] | Input | **Boot Mode 0–1**<br>Determines the MSC8103 boot mode when $\overline{\text{PORESET}}$ is deasserted. See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on how to set these pins. |
| EE4[1] | | **EOnCE Event 4**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EE4 as an input (default) or an output. See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on the ETRSMT Register. |
| | Input | Enable Address Event Detection Channel 4 or generate an EOnCE event. |
| | Output | The DSP wrote the EOnCE Transmit Register (ETRSMT). Triggers external debugging equipment. |
| EE5[1] | | **EOnCE Event 5**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EE5 as an input (default) or an output. |
| | Input | Enable Address Event Detection Channel 5. |
| | Output | Detection by Address Event Detection Channel 5. Triggers external debugging equipment. |
| EED[1] | | **Enhanced OnCE (EOnCE) Event Detection**<br>After $\overline{\text{PORESET}}$ is deasserted, you can configure EED as an input (default) or output: |
| | Input | Enable the Data Event Detection Channel. |
| | Output | Detection by the Data Event Detection Channel. Triggers external debugging equipment. |
| $\overline{\text{PORESET}}$ | Input | **Power-On Reset**<br>When asserted, this line causes the MSC8103 to enter power-on reset state. |
| $\overline{\text{RSTCONF}}$ | Input | **Reset Configuration**<br>Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the "Power-On Reset Flow" and "Hardware Reset Configuration" sections of the *MSC8103 Reference Manual*. |
| $\overline{\text{HRESET}}$ | Input | **Hard Reset**<br>When asserted, this open-drain line causes the MSC8103 to enter the hard reset state. |
| $\overline{\text{SRESET}}$ | Input | **Soft Reset**<br>When asserted, this open-drain line causes the MSC8103 to enter the soft reset state. |
| **Note:** | | See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on how to configure these pins. |

# 1.4 System Bus, HDI16, and Interrupt Signals

The system bus, HDI16, and interrupt signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through registers in the System Interface Unit (SIU) and the Host Interface (HDI16). 1-5 describes the signals in this group.

**Note:** To boot from the host interface, the HDI16 must be enabled by pulling up the HPE signal line during $\overline{\text{PORESET}}$. The configuration word must then be loaded from the host. The configuration word must set the Internal Space Port Size bit in the Bus Control Register (BCR[ISPS]) to change the system data bus width from 64 bits to 32 bits and reassign the upper 32 bits to their HDI16 functions. Never set the Host Port Enable (HEN) bit in the Host Port Control Register (HPCR) to enable the HDI16, unless the bus size is first changed from 64 bits to 32 bits. Otherwise, unpredictable operation may occur.

Although there are eight interrupt request ($\overline{\text{IRQ}}$) connections to the core processor, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration includes two $\overline{\text{IRQ1}}$ and two $\overline{\text{IRQ7}}$ input lines. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions.

**Table 1-5.**    System Bus, HDI16, and Interrupt Signals

| Signal | Data Flow | Description |
|---|---|---|
| A[0–31] | Input/Output | **Address Bus**<br>When the MSC8103 is in external master bus mode, these pins function as the address bus. The MSC8103 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8103 is in Internal Master Bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8103 memory controller. |
| TT[0–4] | Input/Output | **Bus Transfer Type**<br>The bus master drives these pins during the address tenure to specify the type of transaction. |
| TSIZ[0–3] | Input/Output | **Transfer Size**<br>The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction. |
| $\overline{\text{TBST}}$ | Input/Output | **Bus Transfer Burst**<br>The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers four quad words). |
| $\overline{\text{IRQ1}}$ | Input | **Interrupt Request 1**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| $\overline{\text{GBL}}$ | Input/Output | **Global**[1]<br>When a master within the chip initiates a bus transaction, it drives this pin. When an external master initiates a bus transaction, it should drive this pin. Assertion of this pin indicates that the transfer is global and it should be snooped by caches in the system. |
| Reserved | Output | The primary configuration is reserved. |
| BADDR29 | Output | **Burst Address 29**[1]<br>One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| $\overline{\text{IRQ2}}$ | Input | **Interrupt Request 2**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| Reserved | Output | The primary configuration is reserved. |
| BADDR30 | Output | **Burst Address 30**[1]<br>One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| $\overline{\text{IRQ3}}$ | Input | **Interrupt Request 3**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| Reserved | Output | The primary configuration is reserved. |
| BADDR31 | Output | **Burst Address 31**[1]<br>One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| $\overline{\text{IRQ5}}$ | Input | **Interrupt Request 5**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |

**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|---|---|---|
| $\overline{BR}$ | Input/Output<br>Output<br><br><br>Input | **Bus Request**[2]<br>An output when an external arbiter is used. The MSC8103 asserts this pin to request ownership of the bus.<br><br>An input when an internal arbiter is used. An external master should assert this pin to request bus ownership from the internal arbiter. |
| $\overline{BG}$ | Input/Output<br>Output<br><br><br>Input | **Bus Grant**[2]<br>An output when an internal arbiter is used. The MSC8103 asserts this pin to grant bus ownership to an external bus master.<br><br>An input when an external arbiter is used. The external arbiter should assert this pin to grant bus ownership to the MSC8103. |
| $\overline{ABB}$ | Input/Output<br>Output<br><br><br><br>Input | **Address Bus Busy**[1]<br>The MSC8103 asserts this pin for the duration of the address bus tenure. Following an address acknowledge ($\overline{AACK}$) signal, which terminates the address bus tenure, the MSC8103 deasserts $\overline{ABB}$ for a fraction of a bus cycle and then stops driving this pin.<br><br>The MSC8103 does not assume bus ownership while it this pin is asserted by an external bus master. |
| $\overline{IRQ2}$ | Input | **Interrupt Request 2**[1]<br>One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| $\overline{TS}$ | Input/Output | **Bus Transfer Start**<br>Signals the beginning of a new address bus tenure. The MSC8103 asserts this signal when one of its internal bus masters (SC140 core or DMA controller) begins an address tenure. When the MSC8103 senses this pin being asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8103 resources, memory controller support). |
| $\overline{AACK}$ | Input/Output | **Address Acknowledge**<br>A bus slave asserts this signal to indicate that it identified the address tenure. Assertion of this signal terminates the address tenure. |
| $\overline{ARTRY}$ | Input | **Address Retry**<br>Assertion of this signal indicates that the bus transaction should be retried by the bus master. The MSC8103 asserts this signal to enforce data coherency with its internal cache and to prevent deadlock situations. |
| $\overline{DBG}$ | Input/Output<br>Output<br><br><br>Input | **Data Bus Grant**[2]<br>An output when an internal arbiter is used. The MSC8103 asserts this pin as an output to grant data bus ownership to an external bus master.<br><br>An input when an external arbiter is used. The external arbiter should assert this pin as an input to grant data bus ownership to the MSC8103. |
| $\overline{DBB}$ | Input/Output<br>Output<br><br><br>Input | **Data Bus Busy**[1]<br>The MSC8103 asserts this pin as an output for the duration of the data bus tenure. Following a $\overline{TA}$, which terminates the data bus tenure, the MSC8103 deasserts $\overline{DBB}$ for a fraction of a bus cycle and then stops driving this pin.<br><br>The MSC8103 does not assume data bus ownership while $\overline{DBB}$ is asserted by an external bus master. |
| $\overline{IRQ3}$ | Input | **Interrupt Request 3**[1]<br>One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| D[0–31] | Input/Output | **Data Bus Most Significant Word**<br>In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. In Host Port Disabled mode, these 32 bits are part of the 64-bit data bus. In Host Port Enabled mode, these bits are used as the bus in 32-bit mode. |

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**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|--------|-----------|-------------|
| D[32–47] | Input/Output | **Data Bus Bits 32–47**<br>In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. |
| HD[0–15] | Input/Output | **Host Data**[2]<br>When the HDI16 interface is enabled, these signals are lines 0-15 of the bidirectional tri-state data bus. |
| D[48–51] | Input/Output | **Data Bus Bits 48–51**<br>In write transactions the bus master drives the valid data on these pins. In read transactions the slave drives the valid data on these pins. |
| HA[0–3] | Input | **Host Address Line 0–3**[3]<br>When the HDI16 interface bus is enabled, these lines address internal host registers. |
| D52 | Input/Output | **Data Bus Bit 52**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| $\overline{HCS1}$ | Input | **Host Chip Select**[3]<br>When the HDI16 interface is enabled, this is one of the two chip-select pins. The HDI16 chip select is a logical OR of $\overline{HCS1}$ and $\overline{HCS2}$. |
| D53 | Input/Output | **Data Bus Bit 53**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| HRW | Input | **Host Read Write Select**[3]<br>When the HDI16 interface is enabled in Single Strobe mode, this is the read/write input (HRW). |
| $\overline{HRD}$/HRD | Input | **Host Read Strobe**[3]<br>When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the read data strobe Schmitt trigger input ($\overline{HRD}$/HRD). The polarity of the data strobe is programmable. |
| D54 | Input/Output | **Data Bus Bit 54**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| $\overline{HDS}$/HDS | Input | **Host Data Strobe**[3]<br>When the HDI16 is programmed to interface with a single data strobe host bus, this pin is the data strobe Schmitt trigger input ($\overline{HDS}$/HDS). The polarity of the data strobe is programmable. |
| $\overline{HWR}$/HWR | Input | **Host Write Data Strobe**[3]<br>When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the write data strobe Schmitt trigger input ($\overline{HWR}$/HWR). The polarity of the data strobe is programmable. |
| D55 | Input/Output | **Data Bus Bit 55**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| $\overline{HREQ}$/HREQ | Output | **Host Request**[3]<br>When the HDI16 is programmed to interface with a single host request host bus, this pin is the host request output ($\overline{HREQ}$/HREQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output. |
| $\overline{HTRQ}$/HTRQ | Output | **Transmit Host Request**[3]<br>When the HDI16 is programmed to interface with a double host request host bus, this pin is the transmit host request output ($\overline{HTRQ}$/HTRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable. |

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**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|---|---|---|
| D56 | Input/Output | **Data Bus Bit 56**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| HACK/HACK | Output | **Host Acknowledge**[3]<br>When the HDI16 is programmed to interface with a single host request host bus, this pin is the host acknowledge Schmitt trigger input (HACK). The polarity of the host acknowledge is programmable. |
| HRRQ/HRRQ | Output | **Receive Host Request**[3]<br>When the HDI16 is programmed to interface with a double host request host bus, this pin is the receive host request output (HRRQ/HRRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable. |
| D57 | Input/Output | **Data Bus Bit 57**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| HDSP | Input | **Host Data Strobe Polarity**[3]<br>When the HDI16 interface is enabled, this pin is the host data strobe polarity (HDSP). |
| D58 | Input/Output | **Data Bus Bit 58**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| HDDS | Input | **Host Dual Data Strobe**[3]<br>When the HDI16 interface is enabled, this pin is the host dual data strobe (HDDS). |
| D59 | Input/Output | **Data Bus Bit 59**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| H8BIT | Input | **H8BIT**[3]<br>When the HDI16 interface is enabled, this bit determines if the interface is in 8-bit or 16-bit mode. |
| D60 | Input/Output | **Data Bus Bit 60**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| HCS2 | Input | **Host Chip Select** [3]<br>When the HDI16 interface is enabled, this is one of the two chip-select pins. The HDI16 chip select is a logical OR of HCS1 and HCS2. |
| D[61–63] | Input/Output | **Data Bus Bits 61–63**<br>Used only in 60x-mode-only mode. In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. |
| Reserved | | These dedicated signals are reserved when the HDI16 is enabled.**[3]** |
| Reserved | Input | The primary configuration is reserved. |
| DP0 | Input/Output | **Data Parity 0**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity zero pin should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7]. |
| EXT_BR2 | Input | **External Bus Request 2**[1,2]<br>An external master asserts this pin to request bus ownership from the internal arbiter. |

**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|--------|-----------|-------------|
| $\overline{\text{IRQ1}}$ | Input | **Interrupt Request 1**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP1 | Input/Output | **Data Parity 1**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity one pin should give odd parity (odd number of ones) on the group of signals that includes data parity 1 and D[8–15]. |
| $\overline{\text{EXT\_BG2}}$ | Output | **External Bus Grant 2**[1,2]<br>The MSC8103 asserts this pin to grant bus ownership to an external bus master. |
| $\overline{\text{IRQ2}}$ | Input | **Interrupt Request 2**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP2 | Input/Output | **Data Parity 2**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity two pin should give odd parity (odd number of ones) on the group of signals that includes data parity 2 and D[16–23]. |
| $\overline{\text{EXT\_DBG2}}$ | Output | **External Data Bus Grant 2**[1,2]<br>The MSC8103 asserts this pin to grant data bus ownership to an external bus master. |
| $\overline{\text{IRQ3}}$ | Input | **Interrupt Request 3**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP3 | Input/Output | **Data Parity 3**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity three pin should give odd parity (odd number of ones) on the group of signals that includes data parity 3 and D[24–31]. |
| $\overline{\text{EXT\_BR3}}$ | Input | **External Bus Request 3**[1,2]<br>An external master asserts this pin to request bus ownership from the internal arbiter. |
| $\overline{\text{IRQ4}}$ | Input | **Interrupt Request 4**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP4 | Input/Output | **Data Parity 4**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity four pin should give odd parity (odd number of ones) on the group of signals that includes data parity 4 and D[32–39]. |
| DREQ3 | Input | **DMA Request 3**[1]<br>An external peripheral uses this pin to request DMA service. |
| $\overline{\text{EXT\_BG3}}$ | Output | **External Bus Grant 3**[1,2]<br>The MSC8103 asserts this pin to grant bus ownership to an external bus master. |

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**Table 1-5.**    System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|--------|-----------|-------------|
| $\overline{IRQ5}$ | Input | **Interrupt Request 5**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP5 | Input/Output | **Data Parity 5**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity five pin should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47]. |
| DREQ4 | Input | **DMA Request 4**[1]<br>An external peripheral uses this pin to request DMA service. |
| $\overline{EXT\_DBG3}$ | Output | **External Data Bus Grant 3**[1,2]<br>The MSC8103 asserts this pin to grant data bus ownership to an external bus master. |
| $\overline{IRQ6}$ | Input | **Interrupt Request 6**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP6 | Input/Output | **Data Parity 6**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity six pin should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55]. |
| $\overline{DACK3}$ | Output | **DMA Acknowledge 3**[1]<br>The DMA controller drives this output to acknowledge the DMA transaction on the bus. |
| $\overline{IRQ7}$ | Input | **Interrupt Request 7**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP7 | Input/Output | **Data Parity 7**[1]<br>The master or slave that drives the data bus also drives the data parity signals. The value driven on the data parity seven pin should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63]. |
| $\overline{DACK4}$ | Output | **DMA Acknowledge**[1]<br>The DMA controller drives this output to acknowledge the DMA transaction on the bus. |
| $\overline{TA}$ | Input/Output | **Transfer Acknowledge**<br>Indicates that a data beat is valid on the data bus. For single beat transfers, assertion of $\overline{TA}$ indicates the termination of the transfer. For burst transfers, $\overline{TA}$ is asserted four times to indicate the transfer of four data beats with the last assertion indicating the termination of the burst transfer. |
| $\overline{TEA}$ | Input/Output | **Transfer Error Acknowledge**<br>Indicates a bus error. masters within the MSC8103 monitor the state of this pin. The MSC8103 internal bus monitor can assert this pin if it identifies a bus transfer that is hung. |
| $\overline{NMI}$ | Input | **Non-Maskable Interrupt**<br>When an external device asserts this line, the MSC8103 $\overline{NMI}$ input is asserted. |
| NMI_OUT | Output | **Non-Maskable Interrupt**<br>Driven from the MSC8103 internal interrupt controller. Assertion of this output indicates that a non-maskable interrupt, pending in the MSC8103 internal interrupt controller, is waiting to be handled by an external host. |
| $\overline{PSDVAL}$ | Input/Output | **Data Valid**<br>Indicates that a data beat is valid on the data bus. The difference between the $\overline{TA}$ pin and $\overline{PSDVAL}$ is that the $\overline{TA}$ pin is asserted to indicate data transfer terminations while the $\overline{PSDVAL}$ signal is asserted with each data beat movement. Thus, when $\overline{TA}$ is asserted, $\overline{PSDVAL}$ is asserted, but when $\overline{PSDVAL}$ is asserted, $\overline{TA}$ is not necessarily asserted. For example when the SDMA initiates a double word (2x64 bits) transfer to a memory device that has a 32-bit port size, $\overline{PSDVAL}$ is asserted three times without $\overline{TA}$, and finally both pins are asserted to terminate the transfer. |

**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|---|---|---|
| IRQ7 | Input | **Interrupt Request 7**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| INT_OUT | Output | **Interrupt Output**[1]<br>Driven from the MSC8103 internal interrupt controller. Assertion of this output indicates that an unmasked interrupt is pending in the MSC8103 internal interrupt controller. |

**Notes:**
1. See the SIU chapter in the *MSC8103 Reference Manual* for details on how to configure these pins.
2. When used as the bus control arbiter for the system bus, the MSC8103 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals (BR/BG/DBG, EXT_BR2/EXT_BG2/EXT_DBG2, and EXT_BR3/EXT_BG3/EXT_DBG3). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8103 master device. See the Bus Configuration Register (BCR) description in the SIU chapter in the *MSC8103 Reference Manual* for details on how to configure these pins. The second and third set of pins is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of pins (BR/BG/DBG) have a dual function. When the MSC8103 is not the bus arbiter, these signals (BR/BG/DBG) are used by the MSC8103 to obtain master control of the bus.
3. See the host interface (HDI16) chapter in the *MSC8103 Reference Manual* for details on how to configure these pins.

# 1.5 Memory Controller Signals

Refer to the memory controller chapter in the *MSC8103 Reference Manual (MSC8103RM/D)* for detailed information about configuring these signals.

**Table 1-6.** Memory Controller Signals

| Signal | Data Flow | Description |
|---|---|---|
| CS[0–7] | Output | **Chip Select**<br>Enable specific memory devices or peripherals connected to MSC8103 buses. |
| BCTL1 | Output | **Buffer Control 1**<br>Controls buffers on the data bus. Usually used with BCTL0. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See the *System Interface Unit (SIU)* chapter in the *MSC8103 Reference Manual* for details. |
| BADDR[27–28] | Output | **Burst Address 27–28**<br>Two of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| ALE | Output | **Address Latch Enable**<br>Controls the external address latch used in external master bus configuration. |
| BCTL0 | Output | **Buffer Control 0**<br>Controls buffers on the data bus. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See the *System Interface Unit (SIU)* chapter in the *MSC8103 Reference Manual* for details. |
| PWE[0–7] | Output | **Bus Write Enable**<br>Outputs of the bus General-Purpose Chip-select Machine (GPCM). These pins select byte lanes for write operations. |
| PSDDQM[0–7] | Output | **Bus SDRAM DQM**<br>Outputs of the SDRAM control machine. These pins select specific byte lanes of SDRAM devices. |
| PBS[0–7] | Output | **Bus UPM Byte Select**<br>Outputs of the User-Programmable Machine (UPM) in the memory controller. These pins select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device. |

**Table 1-6.** Memory Controller Signals (Continued)

| Signal | Data Flow | Description |
|---|---|---|
| PSDA10 | Output | **Bus SDRAM A10**<br>Output from the bus SDRAM controller. This pin is part of the address when a row address is driven. It is part of the command when a column address is driven. |
| PGPL0 | Output | **Bus UPM General-Purpose Line 0**<br>One of six general-purpose output lines of the UPM. The values and timing of this pin are programmed in the UPM. |
| $\overline{PSDWE}$ | Output | **Bus SDRAM Write Enable**<br>Output from the bus SDRAM controller. This pin should connect to the SDRAM WE input signal. |
| PGPL1 | Output | **Bus UPM General-Purpose Line 1**<br>One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM. |
| $\overline{POE}$ | Output | **Bus Output Enable**<br>Output of the bus GPCM. Controls the output buffer of memory devices during read operations. |
| $\overline{PSDRAS}$ | Output | **Bus SDRAM RAS**<br>Output from the bus SDRAM controller. This pin should connect to the SDRAM Row Address Strobe (RAS) input signal. |
| PGPL2 | Output | **Bus UPM General-Purpose Line 2**<br>One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM. |
| $\overline{PSDCAS}$ | Output | **Bus SDRAM CAS**<br>Output from the bus SDRAM controller. This pin should connect to the SDRAM Column Address Strobe (CAS) input signal. |
| PGPL3 | Output | **Bus UPM General-Purpose Line 3**<br>One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM. |
| $\overline{PGTA}$ | Input | **GPCM TA**<br>Terminates transactions during GPCM operation. Requires an external pull up resistor for proper operation. |
| PUPMWAIT | Input | **Bus UPM Wait**<br>Input to the UPM. An external device can hold this pin high to force the UPM to wait until the device is ready for the operation to continue. |
| $\overline{PPBS}$ | Output | **Bus Parity Byte Select**<br>In systems that store data parity in a separate chip, this output is the byte-select for that chip. |
| PGPL4 | Output | **Bus UPM General-Purpose Line 4**<br>One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM. |
| PSDAMUX | Output | **Bus SDRAM Address Multiplexer**<br>Controls the SDRAM address multiplexer when the MSC8103 is in External Master mode. |
| PGPL5 | Output | **Bus UPM General-Purpose Line 5**<br>One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM. |

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# 1.6  CPM Ports

The MSC8103 CPM supports the subset of MPC8260 signals as described below.

- The MSC8103 CPM includes the following set of communication controllers:
- Two full-duplex fast serial communications controllers (FCCs) that support:
  - Asynchronous transfer mode (ATM) through a UTOPIA 8 interface (FCC1 only)—The MSC8103 can operate as one of the following:
    - UTOPIA slave device
    - UTOPIA multi-PHY master device using direct polling for up to 4 PHY devices
    - UTOPIA multi-PHY master device using multiplex polling that can address up to 31 PHY devices at addresses 0–30 (address 31 is reserved as a null port).
  - IEEE 802.3/Fast Ethernet through a Media-Independent Interface (MII)
  - High-level data link control (HDLC) Protocol:
    - Serial mode—Transfers data one bit at a time
    - Nibble mode—Transfers data four bits at a time
  - Transparent mode serial operation
- One FCC that operates with the TSA only
- Two multi-channel controllers (MCCs) that together can handle up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to four TDM interfaces
- Two full-duplex serial communications controllers (SCCs) that support the following protocols:
  - IEEE 802.3/fast Ethernet through a media-independent interface (MII)
  - HDLC Protocol:
    - Serial mode—Transfers data one bit at a time
    - Nibble mode—Transfers data four bits at a time
  - Synchronous data link control (SDLC)
  - LocalTalk (HDLC-based local area network protocol)
  - Universal asynchronous receiver/transmitter (UART)
  - Synchronous UART (1x clock mode)
  - Binary synchronous (BISYNC) communication
  - Transparent mode serial operation
- Two additional SCCs that operate with the TSA only
- Two full-duplex serial management controllers (SMCs) that support the following protocols:
  - General circuit interface (GCI)/integrated services digital network (ISDN) monitor and C/I channels (TSA only)
  - UART
  - Transparent mode serial operation
- Serial peripheral interface (SPI) support for master or slave operation
- Inter-integrated circuit ($I^2C$) bus controller
- Time-slot assigner (TSA) that supports multiplexing from any of the SCCs, FCCs, SMCs, and two MCCs onto four time-division multiplexed (TDM) interfaces. The TSA uses two serial interfaces (SI1 and SI2). SI1 uses TDMA1 which supports both serial and nibble mode. SI2 does not support nibble mode and includes TDMB2, TDMC2, and TDMD2, which operate only in serial mode.

The individual sets of externals signals associated with a specific protocol and data transfer mode are multiplexed across any or all of the ports, as shown in **Figure 1-2**. The following sections describe the signals supported by Ports A–D.

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# 1.6.1 Port A Signals

**Table 1-7.** Port A Signals

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated Signal** *Protocol* | | |
| PA31 | FCC1: $\overline{\text{TXENB}}$ *UTOPIA master* | Output | **FCC1: UTOPIA Master Transmit Enable** Asserted by the MSC8103 (UTOPIA master PHY) when there is valid transmit cell data (TXD[0–7]). |
| | FCC1: $\overline{\text{TXENB}}$ *UTOPIA slave* | Input | **FCC1: UTOPIA Slave Transmit Enable** Asserted by an external UTOPIA master PHY when there is valid transmit cell data (TXD[0–7]). |
| | FCC1: COL *MII* | Input | **FCC1: Media Independent Interface Collision Detect** Asserted by an external fast Ethernet PHY when collision is detected. |
| PA30 | FCC1: TXCLAV *UTOPIA slave* | Output | **FCC1: UTOPIA Slave Transmit Cell Available** Asserted by the MSC8103 (UTOPIA slave PHY) when the MSC8103 can accept one complete ATM cell. |
| | FCC1: TXCLAV *UTOPIA master*, or | Input | **FCC1: UTOPIA Master Transmit Cell Available** Asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell. |
| | FCC1: TXCLAV0 *UTOPIA master, Multi-PHY, direct polling* | Input | **FCC1: UTOPIA Master Transmit Cell Available Multi-PHY Direct Polling** Asserted by an external UTOPIA slave PHY using direct polling to indicate that it can accept one complete ATM cell. |
| | FCC1: $\overline{\text{RTS}}$ *HDLC, Serial and Nibble* | Output | **FCC1: Request To Send** In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{RTS}}$ is asynchronous with the data. $\overline{\text{RTS}}$ is typically used in conjunction with $\overline{\text{CD}}$. The MSC8103 FCC1 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. |
| | FCC1: CRS *MII* | Input | **FCC1: Media Independent Interface Carrier Sense** Asserted by an external fast Ethernet PHY to indicate activity on the cable. |
| PA29 | FCC1: TXSOC *UTOPIA master* | Output | **FCC1: UTOPIA Transmit Start of Cell** Asserted by the MSC8103 (UTOPIA master PHY) when TXD[0–7] contains the first valid byte of the cell. |
| | FCC1: TX_ER *MII* | Output | **FCC1: Media Independent Interface Transmit Error** Asserted by the MSC8103 to force propagation of transmit errors. |
| PA28 | FCC1: $\overline{\text{RXENB}}$ *UTOPIA master* | Output | **FCC1: UTOPIA Master Receive Enable** Asserted by the MSC8103 (UTOPIA master PHY) to indicate that RXD[0–7] and RXSOC are to be sampled at the end of the next cycle. RXD[0–7] and RXSOC are enabled only in cycles following those with $\overline{\text{RXENB}}$ asserted. |
| | FCC1: $\overline{\text{RXENB}}$ *UTOPIA slave* | Input | **FCC1: UTOPIA Master Receive Enable** Asserted by an external PHY to indicate that RXD[0–7] and RXSOC is to be sampled at the end of the next cycle. RXD[0–7] and RXSOC are enabled only in cycles following those with $\overline{\text{RXENB}}$ asserted. |
| | FCC1: TX_EN *MII* | Output | **FCC1: Media Independent Interface Transmit Enable** Asserted by the MSC8103 when transmitting data. |

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**Table 1-7.** Port A Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated Signal** *Protocol* | | |
| PA27 | FCC1: RXSOC *UTOPIA slave* | Output | **FCC1: UTOPIA Receive Start of Cell** Asserted by the MSC8103 (UTOPIA slave) for an external PHY when RXD[0–7] contains the first valid byte of the cell. |
| | FCC1: RX_DV *MII* | Input | **FCC1: Media Independent Interface Receive Data Valid** Asserted by an external fast Ethernet PHY to indicate that valid data is being sent. The presence of carrier sense but not RX_DV indicates reception of broken packet headers, probably due to bad wiring or a bad circuit. |
| PA26 | FCC1: RXCLAV *UTOPIA slave* | Output | **FCC1: UTOPIA Slave Receive Cell Available** Asserted by the MSC8103 (UTOPIA slave PHY) when one complete ATM cell is available for transfer. |
| | FCC1: RXCLAV *UTOPIA master, or* | Input | **FCC1: UTOPIA Master Receive Cell Available** Asserted by an external PHY when one complete ATM cell is available for transfer. |
| | RXCLAV0 *UTOPIA master, Multi-PHY, direct polling* | Input | **FCC1: UTOPIA Master Receive Cell Available 0 Direct Polling** Asserted by an external PHY when one complete ATM cell is available for transfer. |
| | FCC1: RX_ER *MII* | Input | **FCC1: Media Independent Interface Receive Error** Asserted by an external fast Ethernet PHY to indicate a receive error, which often indicates bad wiring. |
| PA25 | FCC1: TXD0 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 0** The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
| | SDMA: MSNUM0 | Output | **Module Serial Number Bit 0** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |
| PA24 | FCC1: TXD1 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 1** The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 1 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
| | SDMA: MSNUM1 | Output | **Module Serial Number Bit 1** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |
| PA23 | FCC1: TXD2 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 2** The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 2 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |

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**Table 1-7.** Port A Signals (Continued)

| General-Purpose I/O | Peripheral Controller: Dedicated Signal *Protocol* | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| PA22 | FCC1: TXD3 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 3** <br> The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 3 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
| PA21 | FCC1: TXD4 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 4** <br> The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 4 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
|  | FCC1: TXD3 *MII* and *HDLC nibble* | Output | **FCC1: MII and HDLC Nibble Transmit Data Bit 3** <br> TXD[3–0] supports MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. |
| PA20 | FCC1: TXD5 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 5** <br> The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 5 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
|  | FCC1: TXD2 *MII* and *HDLC nibble* | Output | **FCC1: MII and HDLC Nibble Transmit Data Bit 2** <br> TXD[3–0] is supported by MII and HDLC nibble modes in FCC1. This is bit 2 of the transmit data. TXD3 is the most significant bit. |
| PA19 | FCC1: TXD6 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 6** <br> The MSC8103MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 6 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
|  | FCC1: TXD1 *MII* and *HDLC nibble* | Output | **FCC1: MII and HDLC Nibble Transmit Data Bit 1** <br> TXD[3–0] is supported by MII and HDLC transparent nibble modes in FCC1. This is bit 1 of the transmit data. TXD3 is the most significant bit. |
| PA18 | FCC1: TXD7 *UTOPIA* | Output | **FCC1: UTOPIA Transmit Data Bit 7.** <br> The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. |
|  | FCC1: TXD0 *MII* and *HDLC nibble* | Output | **FCC1: MII and HDLC Nibble Transmit Data Bit 0** <br> TXD[3–0] is supported by MII and HDLC nibble modes in FCC1. TXD0 is the least significant bit. |
|  | FCC1: TXD *HDLC serial* and *transparent* | Output | **FCC1: HDLC Serial and Transparent Transmit Data Bit** <br> This is the single transmit data bit in supported by HDLC serial and transparent modes. |

**Table 1-7.** Port A Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated Signal *Protocol* | | |
| PA17 | FCC1: RXD7 *UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 7.** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | FCC1: RXD0 *MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 0** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD0 is the least significant bit. |
| | FCC1: RXD *HDLC serial* and *transparent* | Input | **FCC1: HDLC Serial and Transparent Receive Data Bit** This is the single receive data bit supported by HDLC and transparent modes. |
| PA16 | FCC1: RXD6 *UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 6.** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. This is bit 6 of the receive data. RXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | FCC1: RXD1 *MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 1** This is bit 1 of the receive nibble data. RXD3 is the most significant bit. |
| PA15 | FCC1: RXD5 *UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 5** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. This is bit 5 of the receive data. RXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | RXD2 *MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 2** This is bit 2 of the receive nibble data. RXD3 is the most significant bit. |
| PA14 | FCC1: RXD4 *UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 4.** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | FCC1: RXD3 *MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 3** RXD3 is the most significant bit of the receive nibble bit. |
| PA13 | FCC1: RXD3 *UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 3** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | SDMA: MSNUM2 | Output | **Module Serial Number Bit 2** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |

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**Table 1-7.** Port A Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated Signal *Protocol* | | |
| PA12 | FCC1: RXD2 *UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 2** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. This is bit 2 of the receive data. RXD7 is the most significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | SDMA: MSNUM3 | Output | **Module Serial Number Bit 3** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |
| PA11 | FCC1: RXD1 *UTOPIA* | Input | **FCC1: UTOPIA RX Receive Data Bit 1** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. This is bit 1 of the receive data. RXD7 is the most significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | SDMA: MSNUM4 | Output | **Module Serial Number Bit 4** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |
| PA10 | FCC1: RXD0 *UTOPIA* | Input | **FCC1: UTOPIA RX Receive Data Bit 0** The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD0 is the least significant bit of the receive data. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | SDMA: MSNUM5 | Output | **Module Serial Number Bit 5** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |
| PA9 | SMC2: SMTXD | Output | **SMC2: Serial Management Transmit Data** The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PC15. |
| | SI1 TDMA1: L1TXD0 *TDM nibble* | Output | **Time-Division Multiplexing A1: Layer 1 Transmit Data Bit 0** L1TXD0 is the least significant bit of the TDM nibble data. |
| PA8 | SMC2: SMRXD | Input | **SMC2: Serial Management Receive Data** The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). |
| | SI1 TDMA1: L1RXD0 *TDM nibble* | Input | **Time-Division Multiplexing A1: Layer 1 Nibble Receive Data Bit 0** L1RXD0 is the least significant bit received in nibble mode. |
| | SI1 TDMA1: L1RXD *TDM serial* | Input | **Time-Division Multiplexing A1: Layer 1 Serial Receive Data** TDMA1 receives serial data from L1RXD. |

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**Table 1-7.** Port A Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated Signal *Protocol* | | |
| PA7 | SMC2: SMSYN | Input | **SMC2: Serial Management Synchronization** The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). |
| | SI1 TDMA1: L1TSYNC *TDM nibble* and *TDM serial* | Input | **Time-Division Multiplexing A1: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the *Serial Interface with* time-slot assigner chapter in the *MSC8103 Reference Manual*. |
| PA6 | SI1 TDMA1: L1RSYNC *TDM nibble* and *TDM serial* | Input | **Time-Division Multiplexing A1: Layer 1 Receive Synchronization.** The synchronizing signal for the receive channel. |

# 1.6.2  Port B Signals

**Table 1-8.** Port B Signals

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PB31 | FCC2: TX_ER *MII* | Output | **FCC2: Media Independent Interface Transmit Error** Asserted by the MSC8103 to force propagation of transmit errors. |
| | SCC2: RXD | Input | **SCC2: Receive Data** SCC2 receives serial data from RXD. |
| | SI2 TDMB2: L1TXD *TDM serial* | Output | **Time-Division Multiplexing B2: Layer 1 Transmit Data** TDMB2 transmits serial data out of L1TXD. |
| PB30 | SCC2: TXD | Output | **SCC2: Transmit Data.** SCC2 transmits serial data out of TXD. |
| | FCC2: RX_DV *MII* | Input | **FCC2: Media Independent Interface Receive Data Valid** Asserted by an external fast Ethernet PHY to indicate that valid data is being sent. The presence of carrier sense, but not RX_DV, indicates reception of broken packet headers, probably due to bad wiring or a bad circuit. |
| | SI2 TDMB2: L1RXD *TDM serial* | Input | **Time-Division Multiplexing B2: Layer 1 Receive Data** TDMB2 receives serial data from L1RXD. |
| PB29 | FCC2: TX_EN *MII* | Output | **FCC2: Media Independent Interface Transmit Enable** Asserted by the MSC8103 when transmitting data. |
| | SI2 TDMB2: L1RSYNC *TDM serial* | Input | **Time-Division Multiplexing B2: Layer 1 Receive Synchronization** The synchronizing signal for the receive channel. |

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**Table 1-8.** Port B Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated I/O** *Protocol* | | |
| PB28 | FCC2: RTS<br>*HDLC serial*, *HDLC nibble*, and *transparent* | Output | **FCC2: Request to Send**<br>One of the standard modem interface signals supported by FCC2 (RTS, CTS, and CD). RTS is asynchronous with the data. RTS is typically used in conjunction with CD. The MSC8103 FCC2 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low. |
| | FCC2: RX_ER<br>*MII* | Input | **FCC2: Media Independent Interface Receive Error**<br>Asserted by an external fast Ethernet PHY to indicate a receive error, which often indicates bad wiring. |
| | SCC2: RTS, TENA | Output | **SCC2: Request to Send, Transmit Enable**<br>Typically used in conjunction with CD supported by SCC2. The MSC8103 SCC2 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low. TENA is the signal used in Ethernet mode. |
| | SI2 TDMB2: L1TSYNC<br>*TDM serial* | Input | **Time-Division Multiplexing B2: Layer 1 Transmit Synchronization**<br>The synchronizing signal for the transmit channel. See the serial interface with time-slot assigner chapter in the *MSC8103 Reference Manual*. |
| PB27 | FCC2: COL<br>*MII* | Input | **FCC2: Media Independent Interface Collision Detect**<br>Asserted by an external fast Ethernet PHY when a collision is detected. |
| | SI2 TDMC2: L1TXD<br>*TDM serial* | Output | **Time-Division Multiplexing C2: Layer 1 Transmit Data**<br>TDMC2 transmits serial data out of L1TXD. |
| PB26 | FCC2: CRS<br>*MII* | Input | **FCC2: Media Independent Interface Carrier Sense Input**<br>Asserted by an external fast Ethernet PHY to indicate activity on the cable. |
| | SI2 TDMC2: L1RXD<br>*TDM serial* | Input | **Time-Division Multiplexing C2: Layer 1 Receive Data**<br>TDMC2 receives serial data from L1RXD. |
| PB25 | FCC2: TXD3<br>*MII* and *HDLC nibble* | Output | **FCC2: MII and HDLC Nibble Transmit Data Bit 3**<br>TXD3 is bit 3 and the most significant bit of the transmit data nibble. |
| | SI1 TDMA1: L1TXD3<br>*TDM nibble* | Output | **Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 3**<br>L1TXD3 is bit 3 and the most significant bit of the transmit data nibble. |
| | SI2 TDMC2: L1TSYNC<br>*TDM serial* | Input | **Time-Division Multiplexing C2: Layer 1 Transmit Synchronization**<br>The synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8103 Reference Manual*. |
| PB24 | FCC2: TXD2<br>*MII* and *HDLC nibble* | Output | **FCC2: MII and HDLC Nibble: Transmit Data Bit 2**<br>TXD2 is bit 2 of the transmit data nibble. |
| | SI1 TDMA1: L1RXD3<br>*nibble* | Input | **Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 3**<br>L1RXD3 is bit 3 and the most significant bit of the receive data nibble. |
| | SI2 TDMC2: L1RSYNC<br>*serial* | Input | **Time-Division Multiplexing C2: Layer 1 Receive Synchronization**<br>The synchronizing signal for the receive channel. |

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**Table 1-8.** Port B Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PB23 | FCC2: TXD1 *MII* and *HDLC nibble* | Output | **FCC2: MII and HDLC Nibble: Transmit Data Bit 1** TXD1 is bit 1 of the transmit data nibble. |
| | SI1 TDMA1: L1RXD2 *TDM nibble* | Input | **Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 2** L1RXD2 is bit 2 of the receive data nibble. |
| | SI2 TDMD2: L1TXD *TDM serial* | Output | **Time-Division Multiplexing D2: Layer 1 Transmit Data** TDMA1 transmits serial data out of L1TXD. |
| PB22 | FCC2: TXD0 *MII* and *HDLC nibble* | Output | **FCC2: MII and HDLC Nibble Transmit Data Bit 0** TXD0 is bit 0 and the least significant bit of the transmit data nibble. |
| | FCC2: TXD *HDLC serial* and *transparent* | Output | **FCC2: HDLC Serial and Transparent Transmit Data** Serial data is transmitted via TXD. |
| | SI1 TDMA1: L1RXD1 *TDM nibble* | Input | **Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 1** L1RXD1 is bit 1 of the receive data nibble. |
| | SI2 TDMD2: L1RXD *TDM serial* | Input | **Time-Division Multiplexing D2: Layer 1 Receive Data** Serial data is received via L1RXD. |
| PB21 | FCC2: RXD0 *MII* and *HDLC nibble* | Input | **FCC2: MII and HDLC Nibble Receive Data Bit 0** RXD0 is bit 0 and the least significant bit of the receive data nibble. |
| | FCC2: RXD *HDLC serial* and *transparent* | Input | **FCC2: HDLC Serial and Transparent Receive Data** Serial data is received via RXD. |
| | SI1 TDMA1: L1TXD2 *TDM nibble* | Output | **Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 2** L1TXD2 is bit 2 of the transmit data nibble. |
| | SI2 TDMD2: L1TSYNC *TDM serial* | Input | **Time-Division Multiplexing D2: Layer 1 Transmit Synchronize Data** The synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8103 Reference Manual*. |
| PB20 | FCC2: RXD1 *MII* and *HDLC nibble* | Input | **FCC2: MII and HDLC Nibble: Receive Data Bit 1** RXD1 is bit 1 of the receive data nibble. |
| | SI1 TDMA1: L1TXD1 *TDM nibble* | Output | **Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 1** L1TXD1 is bit 1 of the transmit data nibble. |
| | SI2 TDMD2: L1RSYNC *TDM serial* | Input | **Time-Division Multiplexing D2: Layer 1 Receive Synchronize Data** The synchronizing signal for the receive channel. |
| PB19 | FCC2: RXD2 *MII* and *HDLC nibble* | Input | **FCC2: MII and HDLC Nibble Receive Data Bit 2** RXD2 is bit 2 of the receive data nibble. |
| | $I^2C$: SDA | Input/ Output | **$I^2C$: Inter-Integrated Circuit Serial Data** The $I^2C$ interface comprises two signals: serial data (SDA) and serial clock (SDA). The $I^2C$ controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock. |

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**Table 1-8.** Port B Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PB18 | FCC2: RXD3 *MII* and *HDLC nibble* | Input | **FCC2: MII and HDLC Nibble Receive Data Bit 3** RXD3 is bit 3 and the most significant bit of the receive data nibble. |
| | I²C: SCL | Input/Output | **I²C: Inter-Integrated Circuit Serial Clock** The I²C interface comprises two signals: serial data (SDA) and serial clock (SDA). The I²C controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock. |

# 1.6.3 Port C Signals

**Table 1-9.** Port C Signals

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC31 | BRG1O | Output | **Baud-Rate Generator 1 Output** The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 below), it is the source for BRG1O which is the default input for the SIU timers. See the system interface unit (SIU) chapter in the *MSC8103 Reference Manual* for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 below), the BRG1O input to the SIU timers is disabled. |
| | CLK1 | Input | **Clock 1** The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | TIMER1/2: $\overline{\text{TGATE1}}$ | Input | **Timer 1/2: Timer Gate 1** The timers can be gated/restarted by an external gate signal. There are two gate signals: $\overline{\text{TGATE1}}$ controls timer 1 and/or 2 and $\overline{\text{TGATE2}}$ controls timer 3 and/or 4. |

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**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated I/O** *Protocol* | | |
| PC30 | BRG2O | Output | **Baud-Rate Generator 2 Output**<br>The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. |
| | CLK2 | Input | **Clock 2**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | Timer1: $\overline{\text{TOUT1}}$ | Output | **Timer 1: Timer Out 1**<br>The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer. |
| | EXT1 | Input | **External Request 1**<br>Asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC Controller Configuration Register (RCCR) description in the Chapter 17 of the *MSC8103 Reference Manual* for programming information. There are no current microcode applications for this request line. It is reserved for future development. |
| PC29 | BRG3O | Output | **Baud-Rate Generator 3 Output**<br>The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. |
| | CLK3 | Input | **Clock 3**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | TIN2 | Input | **Timer Input 2**<br>A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges. |
| | SCC1: $\overline{\text{CTS}}$, CLSN | Input | **SCC1: Clear to Send, Collision**<br>Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8103 SCC1 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC15. |

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**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC28 | BRG4O | Output | **Baud-Rate Generator 4 Output** <br> The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. |
| | CLK4 | Input | **Clock 4** <br> The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | TIN1 | Input | **Timer Input 1** <br> A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges. |
| | Timer2: $\overline{\text{TOUT2}}$ | Output | **Timer 2: Timer Output 2** <br> The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT[1–4]}}$) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer. |
| | SCC2: $\overline{\text{CTS}}$, CLSN | Input | **SCC2: Clear to Send, Collision** <br> Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8103 SCC2 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC13. |
| PC27 | BRG5O | Output | **Baud-Rate Generator 5 Output** <br> The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. |
| | CLK5 | Input | **Clock 5** <br> When selected, CLK5 is a source for the SIU timers via BRG1O. See the *System Interface Unit (SIU)* chapter in the *MSC8103 Reference Manual* for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 below), the BRG1O input to the SIU timers is disabled. |
| | TIMER3/4: $\overline{\text{TGATE2}}$ | Input | **Timer 3/4: Timer Gate 2** <br> The timers can be gated/restarted by an external gate signal. There are two gate signals: $\overline{\text{TGATE1}}$ controls timer 1 and/or 2 and $\overline{\text{TGATE2}}$ controls timer 3 and/or 4. |

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**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC26 | BRG6O | Output | **Baud-Rate Generator 6 Output**<br>The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins. |
| | CLK6 | Input | **Clock 6**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | Timer3: $\overline{\text{TOUT3}}$ | Output | **Timer 3: Timer Out 3**<br>The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer. |
| | TMCLK | Input | **Timer Clock**<br>When selected, TMCLK is the designated input to the SIU timers. When TMCLK is configured as the input to the SIU timers, the BRG1O input is disabled. See the *System Interface Unit (SIU)* chapter in the *MSC8103 Reference Manual* for additional information. |
| PC25 | BRG7O | Output | **Baud-Rate Generator 7 Output**<br>The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins. |
| | CLK7 | Input | **Clock 7**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | TIN4 | Input | **Timer Input 4**<br>A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges. |
| | DMA: $\overline{\text{DACK2}}$ | Output | **DMA: Data Acknowledge 2**<br>$\overline{\text{DACK2}}$, $\overline{\text{DREQ2}}$, $\overline{\text{DRACK2}}$ and $\overline{\text{DONE2}}$ belong to the SIU DMA controller. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |

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**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC24 | BRG8O | Output | **Baud-Rate Generator 8 Output**<br>The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. |
| | CLK8 | Input | **Clock 8**<br>The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | TIN3 | Input | **Timer Input 3**<br>A timer can have one of the following sources: another timer, system clock, system clock divided by 16, or a timer input. The CPM supports up to four timer inputs. The timer inputs can be captured on the rising, falling, or both edges. |
| | Timer4: $\overline{\text{TOUT4}}$ | Output | **Timer 4: Timer Out 4**<br>The timers (Timer1–4) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer. |
| | DMA: DREQ2 | Input | **DMA: Data Request 2**<br>$\overline{\text{DACK2}}$, DREQ2, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA controller. DONE2 and DRACK2 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| PC23 | CLK9 | Input | **Clock 9**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | DMA: $\overline{\text{DACK1}}$ | Output | **DMA: Data Acknowledge 1**<br>$\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA controller. DONE1 and DRACK1 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| | EXT2 | Input | **External Request 2**<br>External request input line 2 asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC controller configuration register (RCCR) description in the Chapter 17 of the *MSC8103 Reference Manual* for programming information. There are no current microcode applications for this request line. It is reserved for future development. |

**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC22 | SI1: L1ST1 | Output | **Serial Interface 1: Layer 1 Strobe 1**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | CLK10 | Input | **Clock 10**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | DMA: DREQ1 | Input/ Output | **DMA: Request 1**<br>$\overline{DACK1}$, DREQ1, $\overline{DRACK1}$, and $\overline{DONE1}$ belong to the SIU DMA controller. DONE1 and DRACK1 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| PC15 | SMC2: SMTXD | Output | **SMC2: Serial Management Transmit Data**<br>The SMC interface consists of SMTXD, SMRXD, $\overline{SMSYN}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that support three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PA9. |
| | SCC1: $\overline{CTS}$/CLSN | Input | **SCC1: Clear To Send, Collision**<br>Typically used in conjunction with $\overline{RTS}$. The MSC8103 SCC1 transmitter sends out a request to send data signal ($\overline{RTS}$). The request is accepted when $\overline{CTS}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC29. |
| | FCC1: TXADDR0<br>*UTOPIA master* | Output | **FCC1: UTOPIA Master Transmit Address Bit 0**<br>This is master transmit address bit 0. |
| | FCC1: TXADDR0<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Transmit Address Bit 0**<br>This is slave transmit address bit 0. |
| PC14 | SI1: L1ST2 | Output | **Serial Interface 1: Layer 1 Strobe 2**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also be generate output wave forms for such applications as stepper-motor control. |
| | SCC1: $\overline{CD}$, RENA | Input | **SCC1: Carrier Detect, Receive Enable**<br>Typically used in conjunction with $\overline{RTS}$ supported by SCC1. The MSC8103MSC8103 SCC1 transmitter requests the receiver to send data by asserting $\overline{RTS}$ low. The request is accepted when $\overline{CTS}$ is returned low. |
| | FCC1: RXADDR0<br>*UTOPIA master* | Output | **FCC1: UTOPIA Multi-PHY Master Receive Address Bit 0**<br>This is master receive address bit 0. |
| | FCC1: RXADDR0<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 0**<br>This is slave receive address bit 0. |

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**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC13 | SI1: L1ST4 | Output | **Serial Interface 1: Layer 1 Strobe 4**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | SCC2: $\overline{\text{CTS}}$,CLSN | Input | **SCC2: Clear to Send, Collision**<br>Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8103 SCC2 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC28. |
| | FCC1:TXADDR1<br>*UTOPIA master* | Output | **FCC1: UTOPIA Multi-PHY Master Transmit Address Bit 1**<br>This is master transmit address bit 1. |
| | FCC1: TXADDR1<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Multi-PHY Slave Transmit Address Bit 1**<br>This is slave transmit address bit 1. |
| PC12 | SI1: L1ST3 | Output | **Serial Interface 1: Layer 1 Strobe 3**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | SCC2: $\overline{\text{CD}}$, RENA | Input | **SCC2: Carrier Detect, Request Enable**<br>Typically used in conjunction with $\overline{\text{RTS}}$ supported by SCC2. The MSC8103 SCC2 transmitter requests to the receiver that it sends data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. |
| | FCC1: RXADDR1<br>*UTOPIA master* | Output | **FCC1: UTOPIA Multi-PHY Master Receive Address Bit 1**<br>This is master receive address bit 1. |
| | FCC1: RXADDR1<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 1**<br>This is slave receive address bit 1. |

**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PC7 | SI2: L1ST1 | Output | **Serial Interface 2: Strobe 1**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | FCC1: $\overline{\text{CTS}}$<br>*HDLC serial*, *HDLC nibble*, and *transparent* | Input | **FCC1: Clear To Send**<br>In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data. |
| | FCC1: TXADDR2<br>*UTOPIA master* | Output | **FCC1: UTOPIA Multi-PHY Master Transmit Address Bit 2**<br>This is master transmit address bit 2. |
| | FCC1: TXADDR2<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Multi-PHY Slave Transmit Address Bit 2**<br>This is slave transmit address bit 2. |
| | FCC1: TXCLAV1<br>*UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY Master Transmit Cell Available 1 Direct Polling**<br>Asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell. |
| PC6 | SI2: L1ST2 | Output | **Serial Interface 2: Layer 1 Strobe 2**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | FCC1: $\overline{\text{CD}}$<br>*HDLC serial*, *HDLC nibble*, and *transparent* | Input | **FCC1: Carrier Detect**<br>In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is an input asynchronous with the data. |
| | FCC1: RXADDR2<br>*UTOPIA master* | Output | **FCC1: UTOPIA Multi-PHY Master Receive Address Bit 2**<br>This is master receive address bit 2. |
| | FCC1: RXADDR2<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Receive Address Bit 2**<br>This is slave receive address bit 2. |
| | FCC1: RXCLAV1<br>*UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY Master Receive Cell Available 1 Direct Polling**<br>Asserted by an external PHY when one complete ATM cell is available for transfer. |

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**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated I/O** *Protocol* | | |
| PC5 | SMC1: SMTXD | Output | **SMC1: Transmit Data**<br>The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). |
| | SI2: L1ST3 | Output | **Serial Interface 2: Layer 1 Strobe 3**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | FCC2: $\overline{\text{CTS}}$<br>*HDLC serial*, *HDLC nibble*, and *transparent* | Input | **FCC2: Clear To Send**<br>In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data. |
| PC4 | SMC1: SMRXD | Input | **SMC1: Receive Data**<br>The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). |
| | SI2: L1ST4 | Output | **Serial Interface 2: Layer 1 Strobe 4**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | FCC2: $\overline{\text{CD}}$<br>*HDLC serial*, *HDLC nibble*, and *transparent* | Input | **FCC2: Carrier Detect**<br>In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$ and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is asynchronous with the data. |

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# 1.6.4 Port D Signals

**Table 1-10.** Port D Signals

| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| PD31 | SCC1: RXD | Input | **SCC1: Receive Data**<br>SCC1 receives serial data from RXD. |
| | DMA: DRACK1 | Output | **DMA: Data Request Acknowledge 1**<br>DACK1, DREQ1, DRACK1, and DONE1 belong to the SIU DMA controller. DONE1 and DRACK1 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| | DMA: DONE1 | Input/ Output | **DMA: Done 1**<br>DACK1, DREQ1, DRACK1, and DONE1 belong to the SIU DMA controller. DONE1 and DRACK1 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| PD30 | SCC1: TXD | Output | **SCC1: Transmit Data**<br>SCC1 transmits serial data out of TXD. |
| | DMA: DRACK2 | Output | **DMA: Data Request Acknowledge 2**<br>DACK2, DREQ2, DRACK2, and DONE2 belong to the SIU DMA controller. DONE2 and DRACK2 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| | DMA: DONE2 | Input/ Output | **DMA: Done 2**<br>DACK2, DREQ2, DRACK2, and DONE2 belong to the SIU DMA controller. DONE2 and DRACK2 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| PD29 | SCC1: RTS, TENA | Output | **SCC1: Request to Send, Transmit Enable**<br>Typically used in conjunction with CD supported by SCC2. The MSC8103 SCC1 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low. TENA is the signal used in Ethernet mode. |
| | FCC1: RXADDR3<br>UTOPIA master | Output | **FCC1: UTOPIA Multi-PHY Master Receive Address Bit 3**<br>This is master receive address bit 3. |
| | FCC1: RXADDR3<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Receive Address Bit 3**<br>This is slave receive address bit 3. |
| | FCC1: RXCLAV2<br>*UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY Master Receive Cell Available 2 Direct Polling**<br>Asserted by an external PHY when one complete ATM cell is available for transfer. |

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**Table 1-10.** Port D Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PD19 | FCC1: TXADDR4 *UTOPIA master* | Output | **FCC1: Multi-PHY Master Transmit Address Bit 4 Multiplexed Polling** This is master transmit address bit 4. |
| | FCC1: TXADDR4 *UTOPIA slave* | Input | **FCC1: UTOPIA Slave Transmit Address Bit 4** This is slave transmit address bit 4. |
| | FCC1: TXCLAV3 *UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY master Transmit Cell Available 3 Direct Polling** Asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell. |
| | BRG1O | Output | **Baud Rate Generator 1 Output** The CPM supports up to 8 BRGs for use internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 above), it is the source for BRG1O which is the default input for the SIU timers. See the system interface unit (SIU) chapter in the *MSC8103 Reference Manual* for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 above), the BRG1O input to the SIU timers is disabled. |
| | SPI: $\overline{\text{SPISEL}}$ | Input | **SPI: Select** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select ($\overline{\text{SPISEL}}$). The SPI can be configured as a slave or master in single- or multiple-master environments. $\overline{\text{SPISEL}}$ is the enable input to the SPI slave. In a multimaster environment, $\overline{\text{SPISEL}}$ (always an input) detects an error when more than one master is operating. SPI masters must output a slave select signal to enable SPI slave devices by using a separate general-purpose I/O signal. Assertion of an SPI $\overline{\text{SPISEL}}$ while it is master causes an error. |
| PD18 | FCC1: RXADDR4 *UTOPIA master* | Output | **FCC1: UTOPIA Master Receive Address Bit 4** This is master receive address bit 4. |
| | FCC1: RXADDR4 *UTOPIA slave* | Input | **FCC1: UTOPIA Slave Receive Address Bit 4** This is slave receive address bit 4. |
| | FCC1: RXCLAV3 *UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY Master Receive Cell Available 3 Direct Polling** Asserted by an external PHY when one complete ATM cell is available for transfer. |
| | SPI: SPICLK | Input/ Output | **SPI: Clock** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. SPICLK is a gated clock, active only during data transfers. Four combinations of SPICLK phase and polarity can be configured. When the SPI is a master, SPICLK is the clock output signal that shifts received data in from SPIMISO and transmitted data out to SPIMOSI. |

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**Table 1-10.** Port D Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated I/O** *Protocol* | | |
| PD17 | BRG2O | Output | **Baud Rate Generator 2 Output**<br>The CPM supports up to 8 BRGs for use internally to the MSC8103 and/or to provide an output to one of the 8 BRG pins. |
| | FCC1: RXPRTY<br>*UTOPIA* | Input | **FCC1: UTOPIA Receive Parity**<br>This is the odd parity bit for RXD[0–7]. |
| | SPI: SPIMOSI | Input/ Output | **SPI: Master Output Slave Input**<br>The SPI interface comprises our signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL**).** The SPI can be configured as a slave or master in single- or multiple-master environments. When the SPI is a slave, SPICLK is the clock input that shifts received data in from SPIMOSI and transmitted data out through SPIMISO. |
| PD16 | FCC1: TXPRTY<br>*UTOPIA* | Output | **FCC1: UTOPIA Transmit Parity**<br>This is the odd parity bit for TXD[0–7]. |
| | SPI: SPIMISO | Input/ Output | **SPI: Master Input Slave Output**<br>The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK), and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. When the SPI is a slave, SPICLK is the clock input that shifts received data in from SPIMOSI and transmitted data out through SPIMISO. |
| PD7 | SMC1: $\overline{\text{SMSYN}}$ | Input | **SMC1: Serial Management Synchronization**<br>The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$ and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that support three protocols or modes: UART, transparent or general-circuit interface (GCI). |
| | FCC1: TXADDR3<br>*UTOPIA master* | Output | **FCC1: UTOPIA Master Transmit Address Bit 3**<br>This is master transmit address bit 3. |
| | FCC1: TXADDR3<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Transmit Address Bit 3**<br>This is slave transmit address bit 3. |
| | FCC1: TXCLAV2<br>*UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY Master Transmit Cell Available 2 Direct Polling**<br>Asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell. |

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# 1.7  JTAG Test Access Port Signals

The MSC8103 supports the standard set of Test Access Port (TAP) signals defined by IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-11**.

**Table 1-11.**    JTAG Test Access Port Signals

| Signal Name | Type | Signal Description |
|---|---|---|
| TCK | Input | **Test Clock**<br>A test clock signal for synchronizing JTAG test logic. |
| TDI | Input | **Test Data Input**<br>A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. |
| TDO | Output | **Test Data Output**<br>A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK. |
| TMS | Input | **Test Mode Select**<br>Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor. |
| TRST | Input | **Test Reset**<br>Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up. |

# 1.8  Reserved Signals

**Table 1-12.**    Reserved Signals

| Signal Name | Type | Signal Description |
|---|---|---|
| TEST | Input | **Test**<br>Used for manufacturing testing. You must connect this input to GND. |
| THERM[1–2] | — | Leave disconnected. |
| SPARE1, 5 | — | **Spare Pins**<br>Leave disconnected for backward compatibility with future revisions of this device. |

# Physical and Electrical Specifications    2

This document contains detailed information on environmental limits, power considerations, DC/AC electrical characteristics, and AC timing specifications for the MSC8103 communications processor, mask set 2K87M. For additional information, see the *MSC8103 Reference Manual*.

## 2.1  Absolute Maximum Ratings

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### CAUTION

**This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{CC}$).**

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In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist. **Table 2-1** describes the maximum electrical ratings for the MSC8103.

**Table 2-1.**    Absolute Maximum Ratings[2]

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage[3] | $V_{DD}$ | −0.2 to 1.7 | V |
| PLL supply voltage[3] | $V_{CCSYN}$ | −0.2 to 1.7 | V |
| I/O supply voltage[3] | $V_{DDH}$ | −0.2 to 3.6 | V |
| Input voltage[3] | $V_{IN}$ | (GND − 0.2) to 3.6 | V |
| Maximum operating temperature range[4] | $T_J$ | −40 to 120 | °C |
| Storage temperature range | $T_{STG}$ | −55 to +150 | °C |

Notes:
1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. The input voltage must not exceed the I/O supply $V_{DDH}$ by more than 2.5 V at any time, including during power-on reset. In turn, $V_{DDH}$ can exceed $V_{DD}/V_{CCSYN}$ by more than 3.3 V during power-on reset, but for no more than 100 ms. $V_{DDH}$ should not exceed $V_{DD}/V_{CCSYN}$ by more than 2.1 V during normal operation. $V_{DD}/V_{CCSYN}$ must not exceed $V_{DDH}$ by more than 0.4 V at any time, including during power-on reset. See **Section 4.2**, *Electrical Design Considerations*, on page **4-1** for more information.
4. **Section 4.1**, *Thermal Design Considerations*, on page **4-1** includes a formula for computing the chip junction temperature ($T_J$).

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# 2.2 Recommended Operating Conditions

**Table 2-2** lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 2-2.** Recommended Operating Conditions

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| SC140 core supply voltage | $V_{DD}$ | 275 MHz: 1.5 to 1.7<br>300 MHz: 1.55 to 1.7 | V<br>V |
| PLL supply voltage | $V_{CCSYN}$ | 275 MHz: 1.5 to 1.7<br>300 MHz: 1.55 to 1.7 | V<br>V |
| I/O supply voltage | $V_{DDH}$ | 3.135 to 3.465 | V |
| Input voltage | $V_{IN}$ | −0.2 to $V_{DDH}$ + 0.2 | V |
| Operating temperature range | $T_J$ | 275 MHz: −40 to 105<br>300 MHz: −40 to 75 | °C<br>°C |

# 2.3 Thermal Characteristics

**Table 2-3** describes thermal characteristics of the MSC8103.

**Table 2-3.** Thermal Characteristics

| Characteristic | Symbol | Lidded FC-PBGA 17 × 17 mm | | Unit |
|---|---|---|---|---|
| | | **Natural Convection** | **200 ft/min (1 m/s) airflow** | |
| Junction-to-ambient, single-layer board[1, 2] | $R_{\theta JA}$ or $\theta_{JA}$ | 50 | 37 | °C/W |
| Junction-to-ambient, four-layer board[1, 3] | $R_{\theta JA}$ or $\theta_{JA}$ | 22 | 18 | °C/W |
| Junction-to-board[3] | $R_{\theta JB}$ or $\theta_{JB}$ | 15 | | °C/W |
| Junction-to-case[4] | $R_{\theta JC}$ or $\theta_{JC}$ | 0.8 | | °C/W |

**Notes:**
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-9) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface without thermal grease. TBD = to be determined. If a thin (less than 50 micron) thermal grease interface is established to a heat sink from the lid, the junction to sink thermal resistance is about 0.7 °C/W.

See **Section 4.1**, *Thermal Design Considerations*, on page **4-1** for details on these characteristics.

# 2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8103. The measurements in **Table 2-4** assume the following system conditions:

- $T_J = 0 – 100 \ °C$
- $V_{DD} = 1.6 \ V \pm 5\% \ V_{DC}$
- $V_{DDH} = 3.3 \ V \pm 5\% \ V_{DC}$
- $GND = 0 \ V_{DC}$

**Note:** The leakage current is measured for nominal $V_{DDH}$ and $V_{DD}$ or both $V_{DDH}$ and $V_{DD}$ must vary in the same direction (for example, both $V_{DDH}$ and $V_{DD}$ vary by $\pm 5$ percent).

**Table 2-4.** DC Electrical Characteristics

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage[1], all inputs except CLKIN | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage[1] | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.5 | 3.465 | V |
| CLKIN input low voltage[2] | $V_{ILC}$ | GND | 0.8 | V |
| Input leakage current, $V_{IN} = V_{DDH}$ | $I_{IN}$ | — | 10 | μA |
| Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$ | $I_{OZ}$ | — | 10 | μA |
| Signal low input current[3], $V_{IL} = 0.8 \ V$ | $I_L$ | — | −4.0 | mA |
| Signal high input current[3], $V_{IH} = 2.0 \ V$ | $I_H$ | — | 4.0 | mA |
| Output high voltage, $I_{OH} = −2 \ mA$, except open drain pins | $V_{OH}$ | 2.4 | — | V |
| Output low voltage, $I_{OL} = 3.2 \ mA$ | $V_{OL}$ | — | 0.4 | V |

Notes: 1. See **Figure 2-1** for undershoot and overshoot voltages.
2. The optimum CLKIN duty cycle is obtained when: $V_{ILC} = V_{DDH} – V_{IHC}$.
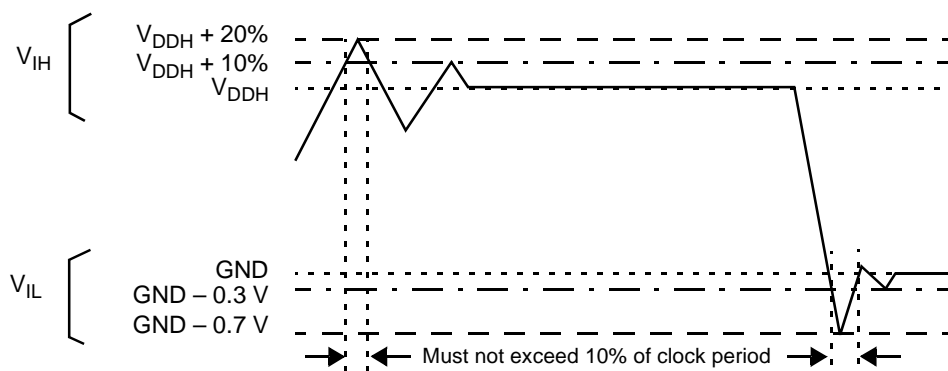3. Not tested. Guaranteed by design.



**Figure 2-1.** Overshoot/Undershoot Voltage for $V_{IH}$ and $V_{IL}$

**Table 2-5.** Typical Power Dissipation

| Characteristic | Symbol | Typical | Unit |
|---|---|---|---|
| Core power dissipation at 300 MHz | $P_{CORE}$ | 450 | mW |
| CPM power dissipation at 200 MHz | $P_{CPM}$ | 320 | mW |
| SIU power dissipation at 100 MHz | $P_{SIU}$ | 80 | mW |
| Core leakage power | $P_{LCO}$ | 3 | mW |
| CPM leakage power | $P_{LCP}$ | 6 | mW |
| SIU leakage power | $P_{LSI}$ | 2 | mW |

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# 2.5 Clock Configuration

The following sections provide a general description of clock configuration.

## 2.5.1 Valid Clock Modes

**Table 2-6** shows the maximum frequency values for each rated core frequency (275 or 300 MHz). The user must ensure that maximum frequency values are not exceeded.

**Table 2-6.** Maximum Frequencies

| Characteristic | Maximum Frequency in MHz | |
|---|---|---|
| Core Frequency | 275 | 300 |
| CPM Frequency (CPMCLK) | 183.33 | 200 |
| Bus Frequency (BCLK) | 91.67 | 100 |
| Serial Communication Controller Clock Frequency (SCLK) | 91.67 | 100 |
| Baud Rate Generator Clock Frequency (BRGCLK) | 91.67 | 100 |
| External Clock Output Frequency (CLKOUT) | 91.67 | 100 |

Six bit values map the MSC8103 clocks to one of the valid configuration mode options. Each option determines the CLKIN, SC140, system bus, SCC clock, CPM, and CLKOUT frequencies. The six bit values are derived from three dedicated input pins (MODCK[1–3]) and three bits from the hard reset configuration word (MODCK_H). To configure the SPLL pre-division factor, SPLL multiplication factor, and the frequencies for the SC140, SCC clocks, CPM parallel I/O ports, and system buses, the MODCK[1–3] pins are sampled and combined with the MODCK_H values when the internal power-on reset (internal $\overline{\text{PORESET}}$) is deasserted. Clock configuration changes only when the internal $\overline{\text{PORESET}}$ signal is deasserted. The following factors are configured:

- SPLL pre-division factor (SPLL PDF)

- SPLL multiplication factor (SPLL MF)

- Bus post-division factor (Bus DF)

- CPM division factor (CPM DF)

- Core division factor (Core DF)

- CPLL pre-division factor (CPLL PDF)

- CPLL multiplication factor (CPLL MF)

The SCC division factor (SCC DF) is fixed at 4. The BRG division factor (BRG DF) is configured through the System Clock Control Register (SCCR) and can be 4, 16 (default after reset), 64, or 256.

**Note:** Refer to *Clock Mode Selection for MSC8101 and MSC8103 Mask Set 2K87M* (AN2306) for details on clock configuration.

## 2.5.2 Clocks Programming Model

This section describes the clock registers in detail. The registers discussed are as follows:

- System Clock Control Register (SCCR)

- System Clock Mode Register (SCMR)

## 2.5.2.1 System Clock Control Register

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | — | | | | | | | | |
| Type | | | | | | | | Reserved | | | | | | | | |
| Reset | | | | | | | | — | | | | | | | | |

| Bit | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | — | | | | | | CLKODIS | | — | | DFBRG |
| Type | | | | | | Reserved | | | | | | R/W | Reserved | | R/W | |
| Reset | | | | | | — | | | | | | 0 | — | | 0 | 1 |

**Figure 2-2.** System Clock Control Register (SCCR)—**0x10C80**

SCCR is memory-mapped into the SIU register map of the MSC8103.

**Table 2-7.** SCCR Bit Descriptions

| Name Bit No. | Defaults | | Description | Settings |
|---|---|---|---|---|
| | **PORESET** | **Hard Reset** | | |
| —<br>0–26 | — | — | Reserved. Write to 0 fro future compatibility. | |
| **CLKODIS**<br>27 | 0 | Unaffected | **CLKOUT Disable**<br>Disables the CLKOUT signal. The value of CLKOUT when disabled is indeterminate (can be 1 or 0). | 0  CLKOUT enabled (default)<br>1  CLKOUT disabled |
| —<br>28–29 | — | — | Reserved. Write to 0 fro future compatibility. | |
| **DFBRG**<br>30–31 | 01 | Unaffected | **Division Factor for the BRG Clock** Defines the BRGCLK frequency. Changing this value does not result in a loss of lock condition. | 00  Divide by 4<br>01  Divide by 16 (default value)<br>10  Divide by 64<br>11  Divide by 256 |

## 2.5.2.2 System Clock Mode Register

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | COREPDF | | | | COREMF | | | | BUSDF | | | | CPMDF | | | |
| Type | | | | | | | | R | | | | | | | | |
| Reset | | | | | | | | — | | | | | | | | |

| Bit | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPLLPDF | | | | SPLLMF | | | | — | DLLDIS | — | | COREDF | | | |
| Type | | | | | | | | R | | | | | | | | |
| Reset | | | | | | | | — | | | | | | | | |

**Figure 2-3.** System Clock Mode Register (SCMR)—**0x10C88**

SCMR is a read-only register that is updated during power-on reset (PORESET) and provides the mode control signals to the PLLs, DLL, and clock logic. This register reflects the currently defined configuration settings. For details of the available setting options, see *AN2306/D*.

**Table 2-8.** SCMR Field Descriptions

| Name Bit No. | Defaults | | Description | Settings |
|---|---|---|---|---|
| | **PORESET** | **Hard Reset** | | |
| **COREPDF** 0–3 | Configuration Pins | Unaffected | **Core PLL Pre-Division Factor** | 0000    CPLL PDF = 1<br>0001    CPLL PDF = 2<br>0010    CPLL PDF = 3<br>0011    CPLL PDF = 4<br>All other combinations not used. |
| **COREMF** 4–7 | Configuration Pins | Unaffected | **Core Multiplication Factor** | 0101    CPLL MF = 10<br>0110    CPLL MF = 12<br>0111    CPLL MF = 14<br>All other combinations not used. |
| **BUSDF** 8–11 | Configuration Pins | Unaffected | **60x-compatible Bus Division Factor** | 0001    Bus DF = 2<br>0010    Bus DF = 3<br>0011    Bus DF = 4<br>0100    Bus DF = 5<br>0101    Bus DF = 6<br>All other combinations not used. |
| **CPMDF** 12–15 | Configuration Pins | Unaffected | **CPM Division Factor** | 0000    CPM DF = 1<br>0001    CPM DF = 2<br>0010    CPM DF = 3<br>All other combinations not used. |
| **SPLLPDF** 16–19 | Configuration Pins | Unaffected | **SPLL Pre-Division Factor** | 0000    SPLL PDF = 1<br>0001    SPLL PDF = 2<br>0010    SPLL PDF = 3<br>0011    SPLL PDF = 4<br>0100    SPLL PDF = 5<br>0101    SPLL PDF = 6<br>All other combinations not used |
| **SPLLMF** 20–23 | Configuration Pins | Unaffected | **SPLL Multiplication Factor** | 0101    SPLL MF = 10<br>0110    SPLL MF = 12<br>0111    SPLL MF = 14<br>1000    SPLL MF = 16<br>1001    SPLL MF = 18<br>1010    SPLL MF = 20<br>1011    SPLL MF = 22<br>1100    SPLL MF = 24<br>1101    SPLL MF = 26<br>1110    SPLL MF = 28<br>1111    SPLL MF = 30<br>All other combinations not used |
| — 24 | — | — | Reserved | |
| **DLLDIS** 25 | Configuration Pins | Unaffected | **DLL Disable** | 0    DLL operation is enabled<br>1    DLL is disabled |
| — 26–27 | — | — | Reserved | |
| **COREDF** 28–31 | Configuration Pins | Unaffected | **Core Division Factor** | 0000    CORE DF = 1<br>0001    CORE DF = 2<br>0010    CORE DF = 3<br>0011    CORE DF = 4<br>0100    CORE DF = 5<br>0101    CORE DF = 6<br>All other combinations not used. |

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# 2.6  AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. AC timings are based on a 50 pF load, except where noted otherwise, and 50 Ω transmission line.

## 2.6.1   Output Buffer Impedances

**Table 2-9.**   Output Buffer Impedances

| Output Buffers | Typical Impedance (Ω) |
|---|---|
| System Bus | 35 |
| Memory Controller | 35 |
| Parallel I/O | 55 |
| **Note:**   These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature. | |

## 2.6.2   Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.6.3** describes the clocking characteristics. **Section 2.6.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8103 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 2-14** for timing.
- If possible, bring up the $V_{DD}$ and $V_{DDH}$ levels together. For designs with separate power supplies, bring up the $V_{DDH}$ levels and then the $V_{DD}$ levels (see **Figure 2-5** and **Figure 2-6**).
- CLKIN can start toggling after $V_{DDH}$ reaches its nominal level, but it must toggle before $V_{DD}$ reaches 0.5 V to guarantee correct device operation (see **Figure 2-4** and **Figure 2-6**).

The following figures show acceptable start-up sequence examples. **Figure 2-4** shows a sequence in which $V_{DD}$ and $V_{DDH}$ are raised together. **Figure 2-5** shows a sequence in which CLKIN starts toggling after $V_{DDH}$ reaches its nominal level and before $V_{DD}$ is applied. **Figure 2-6** shows a sequence in which $V_{DD}$ is raised after $V_{DDH}$ and CLKIN begins to toggle shortly before $V_{DD}$ reaches the 0.5 V level.
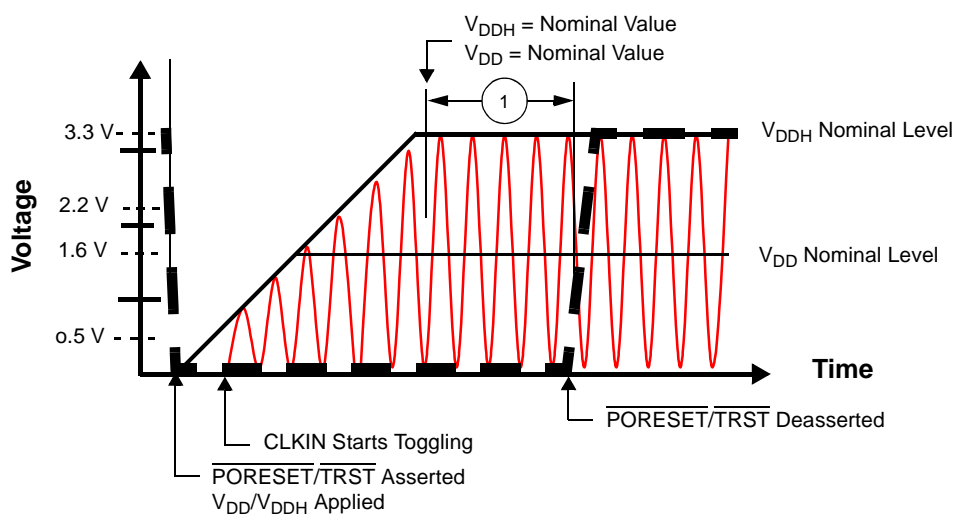


**Figure 2-4.**   Start-Up Sequence with $V_{DD}$ and $V_{DDH}$ Raised Together
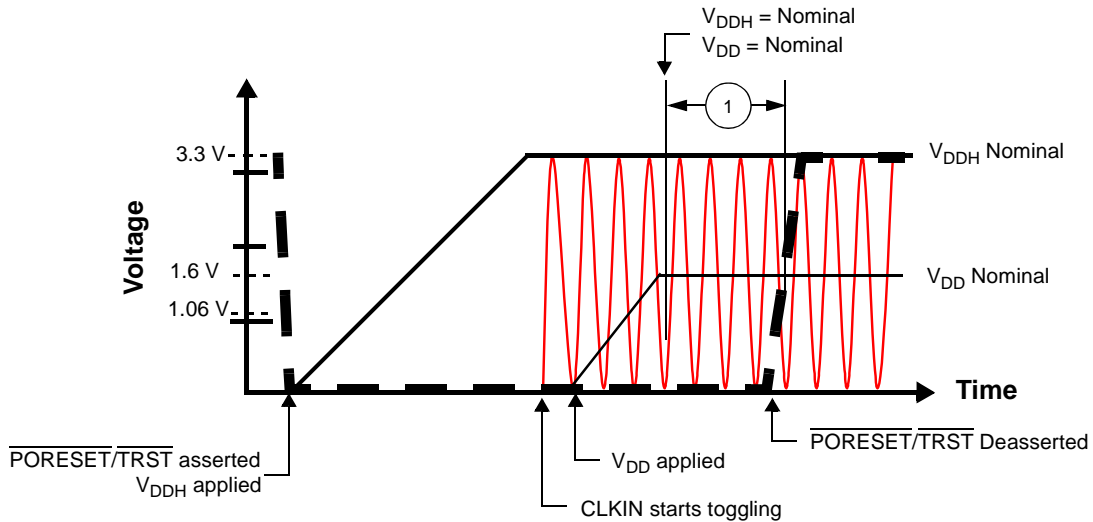
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**Figure 2-5.** Start-Up Sequence with CLKIN Started After $V_{DDH}$ and Before $V_{DD}$
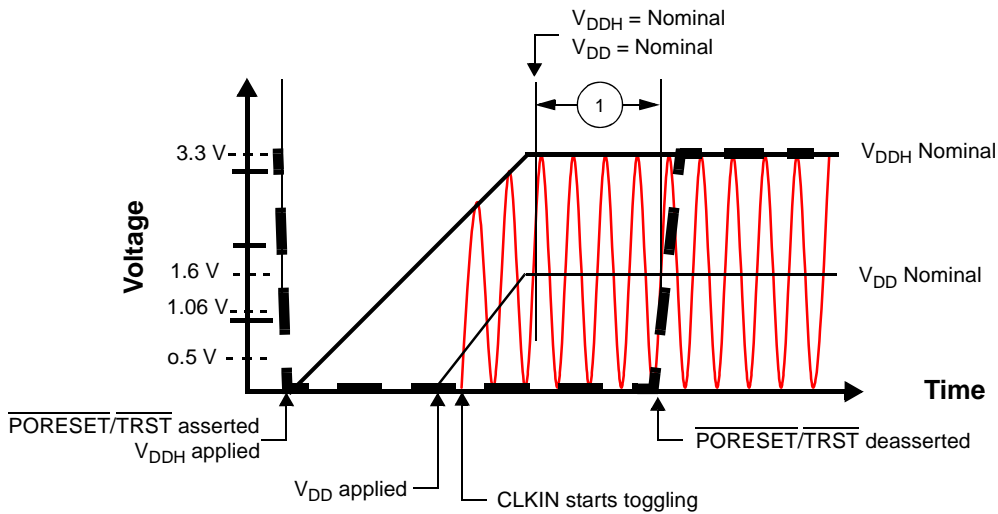


**Figure 2-6.** Start-Up Sequence with $V_{DDH}$ Raised Before $V_{DD}$ with CLKIN Started Before $V_{DD}$ = 0.5 V

# 2.6.3 Clocking and Timing Characteristics

**Table 2-10.** System Clock Parameters

| Characteristic | Minimum | Maximum | Unit |
|---|---|---|---|
| Phase Jitter between BCLK and DLLIN | — | 0.5 | ns |
| CLKIN frequency[1,2] | 18 | 100 | MHz |
| CLKIN slope | — | 5 | ns |
| DLLIN slope | — | 2 | ns |
| CLKOUT frequency jitter | — | (0.01/CLKOUT) + CLKIN jitter | ns |
| Delay between CLKOUT and DLLIN | — | 5 | ns |
| **Notes:** 1. Low CLKIN frequency causes poor PLL performance. Choose a CLKIN frequency high enough to keep the frequency after the predivider (SPLLMFCLK) higher than 18 MHz. <br> 2. CLKIN should have a 50% ± 5% duty cycle. | | | |

**Table 2-11.** Clock Ranges

| Clock | Symbol | Maximum Rated Core Frequency | | |
|---|---|---|---|---|
| | | All | Max. Values for SC140 Clock Rating of: | |
| | | Min | 275 MHz | 300 MHz |
| Input Clock | CLKIN | 18 MHz | 91.67 MHz | 100 MHz |
| SPLL MF Clock | SPLLMFCLK | 18 MHz | 34.38 MHz | 37.5 MHz |
| Bus/Output | BCLK CLKOUT | 18 MHz | 91.67 MHz | 100 MHz |
| Serial Communications Controller | SCLK | 35 MHz | 91.67 MHz | 100 MHz |
| Communications Processor Module | CPMCLK | 70 MHz | 183.3 MHz | 200 MHz |
| SC140 Core | DSPCLK | 72 MHz | 275 MHz | 300 MHz |
| Baud Rate Generator<br>• For BRG DF = 4<br>• For BRG DF = 16 (default)<br>• For BRG DF = 64<br>• For BRG DF = 256 | BRGCLK | 36 MHz<br>9 MHz<br>2.25 MHz<br>562.5 KHz | 91.67 MHz<br>22.91 MHz<br>5.73 MHz<br>1.43 MHz | 100 MHz<br>25 MHz<br>6.25 MHz<br>1.56 MHz |

## 2.6.4 Reset Timing

The MSC8103 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)

- External hard reset ($\overline{\text{HRESET}}$)

- External soft reset ($\overline{\text{SRESET}}$)

Asserting an external $\overline{\text{PORESET}}$ causes concurrent assertion of an internal $\overline{\text{PORESET}}$ signal, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$. When the external $\overline{\text{PORESET}}$ signal is deasserted, the MSC8103 samples several configuration pins:

- $\overline{\text{RSTCONF}}$—determines whether the MSC8103 is a master (0) or slave (1) device

- DBREQ—determines whether to operate in normal mode (0) or invoke the SC140 debug mode (1)

- HPE—disable (0) or enable (1) the host port (HDI16)

- BTM[0–1]—boot from external memory (00) or the HDI16 (01)

All these reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the last sources to cause a reset. **Table 2-12** describes reset causes.

**Table 2-12.** Reset Causes

| Name | Direction | Description |
|---|---|---|
| Power-on reset ($\overline{\text{PORESET}}$) | Input | $\overline{\text{PORESET}}$ initiates the power-on reset flow that resets all the MSC8103s and configures various attributes of the MSC8103, including its clock mode. |
| Hard reset ($\overline{\text{HRESET}}$) | Input/Output | The MSC8103 can detect an external assertion of $\overline{\text{HRESET}}$ only if it occurs while the MSC8103 is not asserting reset. During $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ is asserted. $\overline{\text{HRESET}}$ is an open-drain pin. |
| Soft reset ($\overline{\text{SRESET}}$) | Input/Output | The MSC8103 can detect an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8103 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. |

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## 2.6.4.1  Reset Operation

The reset control logic determines the cause of a reset, synchronizes it if necessary, and resets the appropriate logic modules. The memory controller, system protection logic, interrupt controller, and parallel I/O pins are initialized only on hard reset. Soft reset initializes the internal logic while maintaining the system configuration. The MSC8103 has three mechanisms for reset configuration: host reset configuration, hardware reset configuration, and reduced reset configuration.

## 2.6.4.2  Power-On Reset Flow

Asserting the $\overline{\text{PORESET}}$ external pin initiates the power-on reset flow. $\overline{\text{PORESET}}$ should be asserted externally for at least 16 input clock cycles after external power to the MSC8103 reaches at least 2/3 $V_{CC}$. As **Table 2-13** shows, the MSC8103 has five configuration pins, four of which are multiplexed with the SC140 EONCE Event (EE[0–1], EE[4–5]) pins and the fifth of which is the $\overline{\text{RSTCONF}}$ pin. These pins are sampled at the rising edge of $\overline{\text{PORESET}}$. In addition to these configuration pins, three (MODCK[1–3]) pins are sampled by the MSC8103. The signals on these pins and the MODCK_H value in the Hard Reset Configuration Word determine the PLL locking mode, by defining the ratio between the DSP clock, the bus clocks, and the CPM clock frequencies.

**Table 2-13.**  External Configuration Signals

| Pin | Description | Settings | |
|-----|-------------|----------|---|
| RSTCONF | **Reset Configuration**<br>Input line sampled by the MSC8103 at the rising edge of $\overline{\text{PORESET}}$. | 0<br>1 | Reset Configuration Master.<br>Reset Configuration Slave. |
| DBREQ/ EE0 | **EONCE Event Bit 0**<br>Input line sampled after SC140 core PLL locks. Holding EE0 high when $\overline{\text{PORESET}}$ is deasserted puts the SC140 into Debug mode. | 0<br><br>1 | SC140 starts the normal processing mode after reset.<br>SC140 enters Debug mode immediately after reset. |
| HPE/EE1 | **Host Port Enable**<br>Input line sampled at the rising edge of $\overline{\text{PORESET}}$. If asserted, the Host port is enabled, the system data bus is 32-bit wide, and the Host *must* program the reset configuration word. | 0<br><br>1 | Host port disabled (hardware reset configuration enabled).<br>Host port enabled. |
| BTM[0–1]/ EE[4–5] | **Boot Mode**<br>Input lines sampled at the rising edge of $\overline{\text{PORESET}}$, which determine the MSC8103 Boot mode. | 00<br>01<br>10<br>11 | MSC8103 boots from external memory.<br>MSC8103 boots from HDI16.<br>Reserved.<br>Reserved. |

**Table 2-14.**  Reset Timing

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|-----------------|------------|-----|-----|------|
| 1 | Required external $\overline{\text{PORESET}}$ duration minimum<br>• CLKIN = 18 MHz<br>• CLKIN = 75 MHz | 16 / CLKIN | <br>888.8<br>213.3 | <br>—<br>— | <br>ns<br>ns |
| 2 | Delay from deassertion of external $\overline{\text{PORESET}}$ to deassertion of internal $\overline{\text{PORESET}}$<br>• CLKIN = 18 MHz<br>• CLKIN = 75 MHz | 1024 / CLKIN | <br><br>56.89<br>13.65 | | <br><br>µs<br>µs |
| 3 | Delay from deassertion of internal $\overline{\text{PORESET}}$ to SPLL lock<br>• SPLLMFCLK = 18 MHz<br>• SPLLMFCLK = 25 MHz | 800 / SPLLMFCLK | <br>44.4<br>32.0 | | <br>µs<br>µs |

**Table 2-14.**  Reset Timing (Continued)

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|-----------------|------------|-----|-----|------|
| 4 | Delay from SPLL lock to DLL lock<br>• DLL enabled<br>— BCLK = 18 MHz<br>— BCLK = 75 MHz<br>• DLL disabled | 3073 / BLCK<br><br><br><br>— | | 170.72<br>40.97<br>0.0 | µs<br>µs<br>ns |
| 5 | Delay from SPLL lock to $\overline{\text{HRESET}}$ deassertion<br>• DLL enabled<br>— BCLK = 18 MHz<br>— BCLK = 75 MHz<br>• DLL disabled<br>— BCLK = 18 MHz<br>— BCLK = 75 MHz | 3585 / BLCK<br><br><br><br>512 / BLCK | | 199.17<br>47.5<br><br>28.4<br>6.83 | µs<br>µs<br><br>µs<br>µs |
| 6 | Delay from SPLL lock to $\overline{\text{SRESET}}$ deassertion<br>• DLL enabled<br>— BCLK = 18 MHz<br>— BCLK = 75 MHz<br>• DLL disabled<br>— BCLK = 18 MHz<br>— BCLK = 75 MHz | 3588 / BLCK<br><br><br><br>515 / BLCK | | 199.33<br>47.84<br><br>28.61<br>6.87 | µs<br>µs<br><br>µs<br>µs |
| **Note:** | Value given for lowest possible CLKIN frequency 18 MHz to ensure proper initialization of reset sequence. | | | | |

## 2.6.4.3  Host Reset Configuration

Host reset configuration allows the host to program the reset configuration word via the Host port after $\overline{\text{PORESET}}$ is deasserted, as described in the *MSC8103 Reference Manual*. The MSC8103 samples the signals described in **Table 2-13** one the rising edge of $\overline{\text{PORESET}}$ when the signal is deasserted.

If HPE is sampled high, the host port is enabled. In this mode the $\overline{\text{RSTCONF}}$ pin *must* be pulled up. The device extends the internal $\overline{\text{PORESET}}$ until the host programs the reset configuration word register. The host must write four 8-bit half-words to the Host Reset Configuration Register address to program the reset configuration word, which is 32 bits wide. For more information, see the *MSC8103 Reference Manual*. The reset configuration word is programmed before the internal PLL and DLL in the MSC8103 are locked. The host must program it after the rising edge of the $\overline{\text{PORESET}}$ input. In this mode, the host must have its own clock that does not depend on the MSC8103 clock. After the PLL and DLL are locked, $\overline{\text{HRESET}}$ remains asserted for another 512 bus clocks and is then released. The $\overline{\text{SRESET}}$ is released three bus clocks later (see **Figure 2-7**).
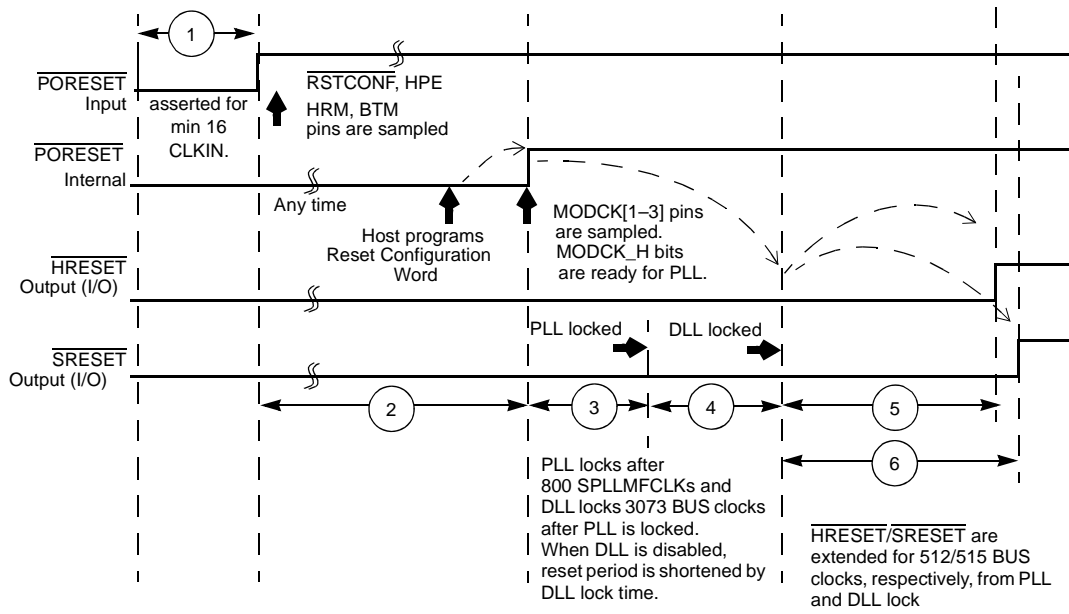
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**Figure 2-7.**   Host Reset Configuration Timing

## 2.6.4.4 Hardware Reset Configuration

Hardware reset configuration is enabled if HPE is sampled low at the rising edge of $\overline{\text{PORESET}}$. The value driven on $\overline{\text{RSTCONF}}$ while $\overline{\text{PORESET}}$ changes from assertion to deassertion determines the MSC8103 configuration. If $\overline{\text{RSTCONF}}$ is deasserted (driven high) while $\overline{\text{PORESET}}$ changes, the MSC8103 acts as a configuration slave. If $\overline{\text{RSTCONF}}$ is asserted (driven low) while $\overline{\text{PORESET}}$ changes, the MSC8103 acts as a configuration master. **Section 2.6.4.4**, *Hardware Reset Configuration*, explains the configuration sequence and the terms "configuration master" and "configuration slave."

Directly after the deassertion of $\overline{\text{PORESET}}$ and choice of the reset operation mode as configuration master or configuration slave, the MSC8103 starts the configuration process. The MSC8103 asserts $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ throughout the power-on reset process, including configuration. Configuration takes 1024 CLOCKIN cycles, after which MODCK[1–3] are sampled to determine the MSC8103's working mode.

Next, the MSC8103 halts until the SPLL locks. The SPLL locks according to MODCK[1–3], which are sampled, and to MODCK_H taken from the Reset Configuration Word. SPLL locking time is 800 reference clocks, which is the clock at the output of the SPLL Pre-divider. After the SPLL is locked, all the clocks to the MSC8103 are enabled. If the DLLDIS bit in the reset configuration word is reset, the DLL starts the locking process after the SPLL is locked. During PLL and DLL locking, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are asserted. $\overline{\text{HRESET}}$ remains asserted for another 512 BUS clocks and is then released. The $\overline{\text{SRESET}}$ is released three bus clocks later. If the DLLDIS bit in the reset configuration word is set, the DLL is bypassed and there is no locking process, thus saving the DLL locking time. **Figure 2-8** shows the power-on reset flow.
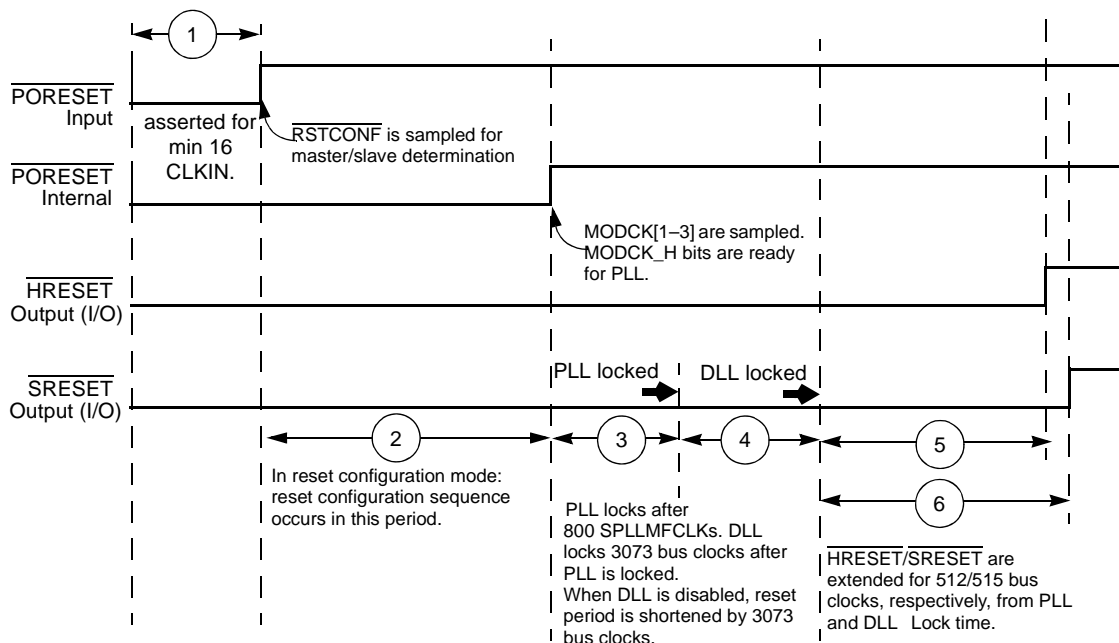


**Figure 2-8.**   Hardware Reset Configuration Timing

# 2.6.5   System Bus Access Timing

## 2.6.5.1   Core Data Transfers

Generally, all MSC8103 bus and system output signals are driven from the rising edge of the reference clock (REFCLK), which is DLLIN. Memory controller signals, however, trigger on four points within a DLLIN cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of DLLIN (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2-15** shows.

**Table 2-15.**    Tick Spacing for Memory Controller Signals

| PLL Clock Ratio | Tick Spacing (T1 Occurs at the Rising Edge of DLLIN) | | |
|---|---|---|---|
| | **T2** | **T3** | **T4** |
| 1:2, 1:3, 1:4, 1:5, 1:6 | 1/4 DLLIN | 1/2 DLLIN | 3/4 DLLIN |
| 1:2.5 | 3/10 DLLIN | 1/2 DLLIN | 8/10 DLLIN |
| 1:3.5 | 4/14 DLLIN | 1/2 DLLIN | 11/14 DLLIN |

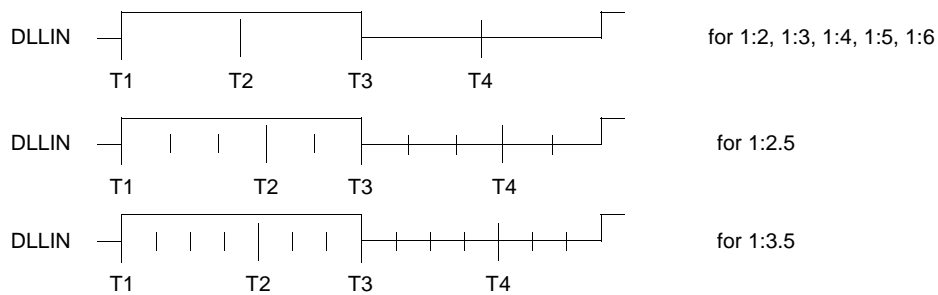**Figure 2-9** is a graphical representation of **Table 2-15**.



**Figure 2-9.**    Internal Tick Spacing for Memory Controller Signals

**Note:**   The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. SDRAM machine outputs change only on the DLLIN rising edge.

**Table 2-16.** AC Timing for SIU Inputs

| No. | Characteristic | Value[2] | Units |
|---|---|---|---|
| 10 | Hold time for all signals after the 50% level of the DLLIN rising edge | 0.5 | ns |
| 11a | $\overline{ABB}/\overline{AACK}$ set-up time before the 50% level of the DLLIN rising edge | 3.5 | ns |
| 11b | $\overline{DBG}/\overline{DBB}/\overline{BR}/\overline{TC}$ set-up time before the 50% level of the DLLIN rising edge | 5.0 | ns |
| 11c | $\overline{ARTRY}$ set-up time before the 50% level of the DLLIN rising edge | 4.0 | ns |
| 11d | $\overline{TA}$ set-up time before the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>3.5<br>4.0 | <br>ns<br>ns |
| 11e | $\overline{TEA}$ set-up time before the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>4.0<br>3.0 | <br>ns<br>ns |
| 11f | $\overline{PSDVAL}$ set-up time before the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>3.5<br>3.5 | <br>ns<br>ns |
| 11g | $\overline{TS}$ set-up time before the 50% level of the DLLIN rising edge | 5.0 | ns |
| 11h | $\overline{BG}$ set-up time before the 50% level of the DLLIN rising edge | 4.5 | ns |
| 12 | Data bus set-up time before the 50% level of the DLLIN rising edge in Normal<br>• Pipeline mode<br>• Non-pipeline mode | <br>2.5<br>5.0 | <br>ns<br>ns |
| 13 | Data bus set-up time before the 50% level of the DLLIN rising edge in ECC and PARITY modes<br>• Pipeline mode<br>• Non-pipeline mode | <br><br>2.5<br>8.0 | <br><br>ns<br>ns |
| 14 | DP set-up time before the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>4.0<br>9.0 | <br>ns<br>ns |
| 15a | Address bus set-up time before the 50% level of the DLLIN rising edge<br>• Extra cycle mode (SIUBCR[EXDD] = 0)<br>• Non-extra cycle mode (SIUBCR[EXDD] = 1) | <br>5.0<br>8.0 | <br>ns<br>ns |
| 15b | Address attributes: TT/$\overline{TBST}$/TSIZ/$\overline{GBL}$ set-up time before the 50% level of the DLLIN rising edge<br>• Extra cycle mode (SIUBCR[EXDD] = 0)<br>• Non-extra cycle mode (SIUBCR[EXDD] = 1) | <br><br>5.0<br>5.5 | <br><br>ns<br>ns |
| 16[1] | PUPMWAIT/$\overline{IRQ}$ signals set-up time before the 50% level of the DLLIN rising edge | 3.0 | ns |

**Notes:** 1. The set-up time for these signals is for synchronous operation. Any set-up time can be used for asynchronous operation.
2. Input specifications are measured from the 50% level of the rising edge of DLLIN to the 50% level of the signal. Timings are measured at the pin.

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**Table 2-17.** AC Timing for SIU Outputs

| No. | Characteristic | Min. | Maximum[2] | | Units |
|---|---|---|---|---|---|
| | | | 30 pF | 50 pF | |
| 31a | $\overline{\text{TA}}$ delay from the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>1.0<br>1.0 | <br>5.0<br>4.0 | <br>6.5<br>5.5 | <br>ns<br>ns |
| 31b | $\overline{\text{TEA}}$ delay from the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>1.0<br>1.0 | <br>3.0<br>3.5 | <br>4.5<br>5.0 | <br>ns<br>ns |
| 31c | $\overline{\text{PSDVAL}}$ delay from the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>1.0<br>1.0 | <br>4.0<br>3.5 | <br>5.5<br>5.0 | <br>ns<br>ns |
| 32a | Address bus delay from the 50% level of the DLLIN rising edge<br>• Multi master mode (SIUBCR[EBM] = 1)<br>• Single master mode (SIUBCR[EBM] = 0) | <br>1.0<br>1.0 | <br>6.3<br>5.5 | <br>7.8<br>7.0 | <br>ns<br>ns |
| 32b | Address attributes: TT/$\overline{\text{TBST}}$/TSIZ/$\overline{\text{GBL}}$ delay from the 50% level of the DLLIN rising edge | 1.0 | 5.5 | 7.0 | ns |
| 32c | BADDR delay from the 50% level of the DLLIN rising edge | 1.0 | 3.5 | 5.0 | ns |
| 33a | Data bus delay from the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>1.0<br>1.0 | <br>5.0<br>6.0 | <br>6.5<br>7.5 | <br>ns<br>ns |
| 33b | DP delay from the 50% level of the DLLIN rising edge<br>• Pipeline mode<br>• Non-pipeline mode | <br>1.0<br>1.0 | <br>4.0<br>6.5 | <br>5.5<br>8.0 | <br>ns<br>ns |
| 34 | Memory controller signals/ALE delay from the 50% level of the DLLIN rising edge | 1.0 | 5.5 | 7.0 | ns |
| 35a | $\overline{\text{DBG}}$/$\overline{\text{BR}}$/$\overline{\text{DBB}}$ delay from the 50% level of the DLLIN rising edge | 1.0 | 4.0 | 5.5 | ns |
| 35b | $\overline{\text{AACK}}$/$\overline{\text{ABB}}$/$\overline{\text{CS}}$ delay from the 50% level of the DLLIN rising edge | 1.0 | 4.5 | 6.0 | ns |
| 35c | $\overline{\text{BG}}$ delay from the 50% level of the DLLIN rising edge | 1.0 | 4.0 | 5.5 | ns |
| 35d | $\overline{\text{TS}}$ delay from the 50% level of the DLLIN rising edge | 1.0 | 3.5 | 5.0 | ns |
| 36 | Delay from the 50% level of the DLLIN rising edge for all other signals | 1.0 | 4.5 | 6.0 | ns |

Notes:
1. The maximum bus frequency depends on the mode:
   • In 60x-compatible mode connected to another MSC8103 device, the frequency is determined by adding the input and output longest timing values, which results in a frequency of 75 MHz for 30 pF output capacitance. In multi-master mode when connected to another MSC8103 device, the frequency is determined by adding the input and output longest timing values, which results in a frequency of 75 MHz for 30 pF output capacitance.
   • Certain bus modes, such as non-extra cycle (EXDD = 1), non-pipelined, and ECC/Parity modes, result in slower bus frequencies.
   • In single-master mode, the frequency depends on the timing of the devices connected to the MSC8103.
2. Output specifications are measured from the 50% level of the rising edge of DLLIN to the 50% level of the signal. Timings are measured at the pin.

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DLLIN

$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$
PSDVAL/ABB/DBB/$\overline{\text{TS}}$ inputs

Data bus inputs—normal mode

Data bus inputs—ECC and parity modes

DP inputs

Address bus/TT[0–4]/TC[0–2]/$\overline{\text{TBST}}$/TSIZ[0–3]/$\overline{\text{GBL}}$ inputs

PUPMWAIT/$\overline{\text{IRQn}}$ input

$\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ outputs

Address bus/TT[0–4]/TC[0–2]/$\overline{\text{TBST}}$/TSIZ[0–3]/$\overline{\text{GBL}}$/BADDR[27–31] outputs

Data bus outputs

DP outputs

Memory controller/ALE signals

$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{ABB}}$/$\overline{\text{TS}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{DBB}}$/$\overline{\text{CS}}$ signals
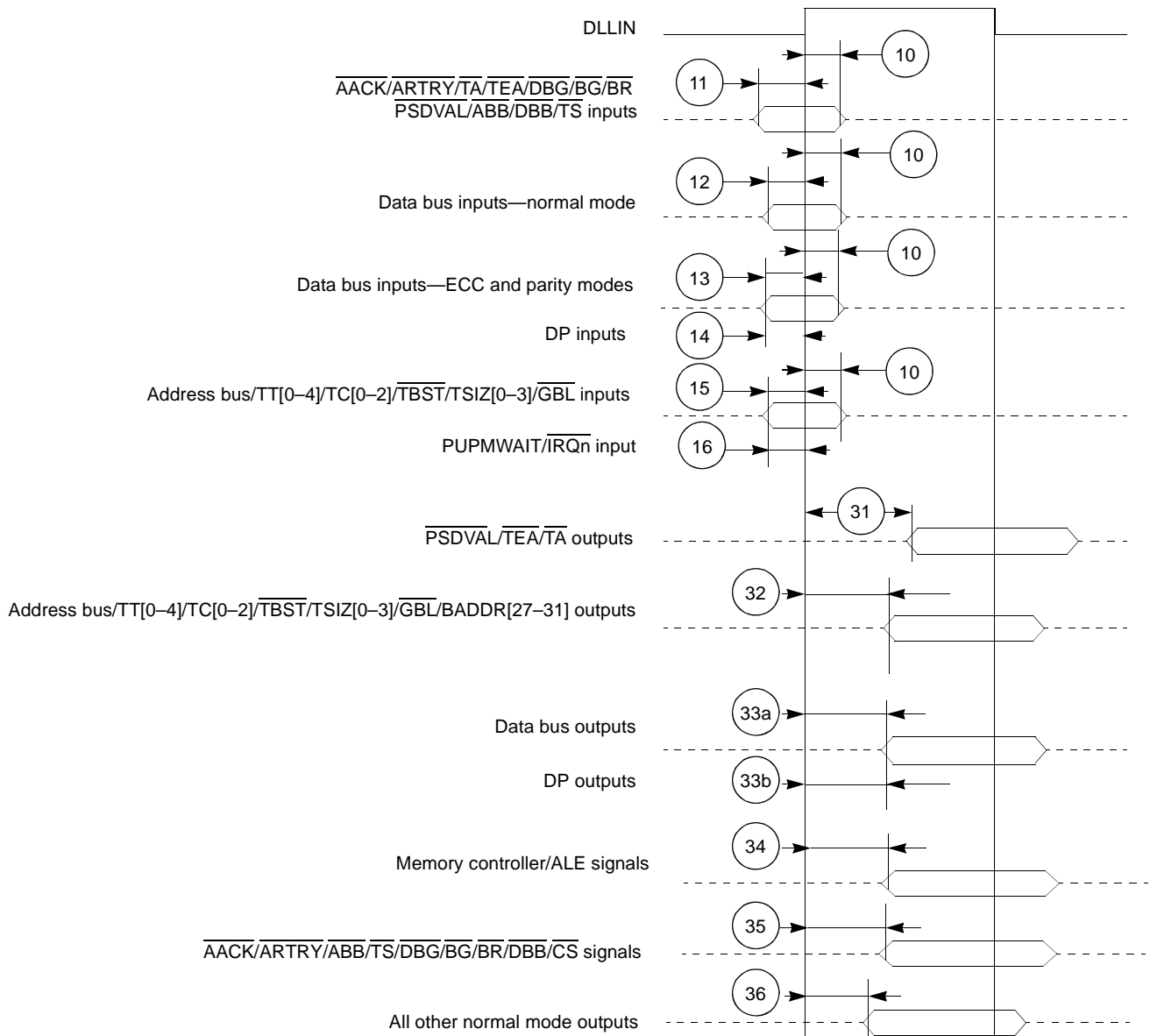
All other normal mode outputs

**Figure 2-10.** Bus Signal Timing

## 2.6.5.2  DMA Data Transfers

**Table 2-18** describes the DMA signal timing.

**Table 2-18.**    DMA Signals

| Number | Characteristic | Minimum | Maximum | Units |
|--------|----------------|---------|---------|-------|
| 72 | DREQ set-up time before DLLIN falling edge | 6 | — | ns |
| 73 | DREQ hold time after DLLIN falling edge | 0.5 | — | ns |
| 74 | $\overline{\text{DONE}}$ set-up time before DLLIN rising edge | 9 | — | ns |
| 75 | $\overline{\text{DONE}}$ hold time after DLLIN rising edge | 0.5 | — | ns |
| 76 | $\overline{\text{DACK}}/\overline{\text{DRACK}}/\overline{\text{DONE}}$ delay after DLLIN rising edge | 0.5 | 9 | ns |

The DREQ signal is synchronized with the falling edge of DLLIN. $\overline{\text{DONE}}$ timing is relative to the rising edge of DLLIN. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-18**. **Figure 2-11** shows synchronous peripheral interaction.
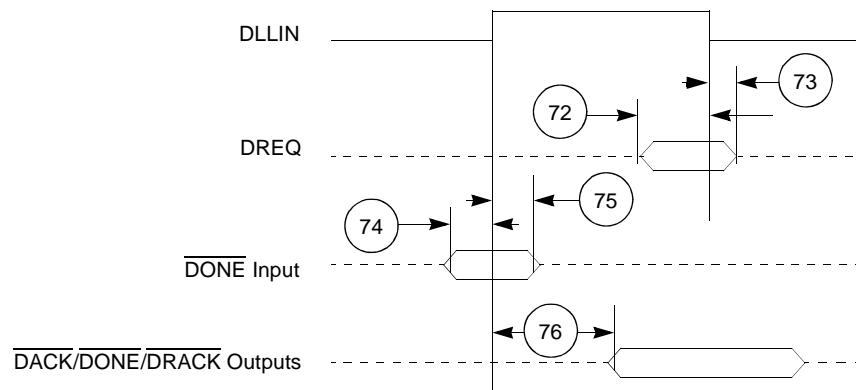


**Figure 2-11.**    DMA Signals

## 2.6.6  HDI16 Signals

**Table 2-19.**    Host Interface (HDI16) Timing[1, 2]

| Number | Characteristics[3] | Expression | Value | Unit |
|--------|---------------------|------------|-------|------|
| 44a | Read data strobe minimum assertion width[4] <br> $\overline{\text{HACK}}$ read minimum assertion width | $(1.5 \times T_C) + 5.0$ | Note 11 | ns |
| 44b | Read data strobe minimum deassertion width[4] <br> $\overline{\text{HACK}}$ read minimum deassertion width | $T_C + 5.0$ | Note 11 | ns |
| 44c | Read data strobe minimum deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] <br> $\overline{\text{HACK}}$ minimum deassertion width after "Last Data Register" reads[5,6] | $(2.5 \times T_C) + 5.0$ | Note 11 | ns |
| 45 | Write data strobe minimum assertion width[8] <br> $\overline{\text{HACK}}$ write minimum assertion width | $(1.5 \times T_C) + 5.0$ | Note 11 | ns |
| 46 | Write data strobe minimum deassertion width[8] <br> $\overline{\text{HACK}}$ write minimum deassertion width after ICR, CVR and Data Register writes[5] | $(2.5 \times T_C) + 5.0$ | Note 11 | ns |
| 47 | Host data input minimum set-up time before write data strobe deassertion[8] <br> Host data input minimum set-up time before $\overline{\text{HACK}}$ write deassertion | — | 5.0 | ns |

**Table 2-19.** Host Interface (HDI16) Timing[1, 2] (Continued)

| Number | Characteristics[3] | Expression | Value | Unit |
|:---:|---|:---:|:---:|:---:|
| 48 | Host data input minimum hold time after write data strobe deassertion[8]<br>Host data input minimum hold time after $\overline{\text{HACK}}$ write deassertion | — | 5.0 | ns |
| 49 | Read data strobe minimum assertion to output data active from high impedance[4]<br>$\overline{\text{HACK}}$ read minimum assertion to output data active from high impedance | — | 5.0 | ns |
| 50 | Read data strobe maximum assertion to output data valid[4]<br>$\overline{\text{HACK}}$ read maximum assertion to output data valid | $(2.0 \times T_C) + 5.0$ | Note 11 | ns |
| 51 | Read data strobe maximum deassertion to output data high impedance[4]<br>$\overline{\text{HACK}}$ read maximum deassertion to output data high impedance | — | 5.0 | ns |
| 52 | Output data minimum hold time after read data strobe deassertion[4]<br>Output data minimum hold time after $\overline{\text{HACK}}$ read deassertion | — | 5.0 | ns |
| 53 | HCS[1–2] minimum assertion to read data strobe assertion[4] | — | 5.0 | ns |
| 54 | HCS[1–2] minimum assertion to write data strobe assertion[8] | — | 5.0 | ns |
| 55 | HCS[1–2] maximum assertion to output data valid | $T_C + 5.0$ | Note 11 | ns |
| 56 | HCS[1–2] minimum hold time after data strobe deassertion[9] | — | 0.0 | ns |
| 57 | HA[0–3], HRW minimum set-up time before data strobe assertion[9]<br>• Read<br>• Write | — | 0<br>5.0 | ns<br>ns |
| 58 | HA[0–3], HRW minimum hold time after data strobe deassertion[9] | — | 5.0 | ns |
| 61 | Maximum delay from read data strobe deassertion to host request deassertion for "Last Data Register" read[4, 5, 10] | $(3.5 \times T_C) + 5.0$ | Note 11 | ns |
| 62 | Maximum delay from write data strobe deassertion to host request deassertion for "Last Data Register" write[5,8,10] | $(3.0 \times T_C) + 5$ | Note 11 | ns |
| 63 | Minimum delay from DMA $\overline{\text{HACK}}$ (OAD=0) or Read/Write data strobe(OAD=1) deassertion to $\overline{\text{HREQ}}$ assertion. | $(5.0 \times T_C) + 5.0$ | Note 11 | ns |
| 64 | Maximum delay from DMA $\overline{\text{HACK}}$ (OAD=0) or Read/Write data strobe(OAD=1) assertion to $\overline{\text{HREQ}}$ deassertion | $(3.5 \times T_C) + 5.0$ | Note 11 | ns |

**Notes:** 
1. $T_C$ = 1/ DSPCLK. At 300 MHz, $T_C$ = 3.3 ns
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. $V_{CC}$ = 3.3 V ± 0.3 V; $T_J$ = –40°C to +100 °C, $C_L$ = 50 pF
4. The read data strobe is $\overline{\text{HRD}}$/HRD in the dual data strobe mode and $\overline{\text{HDS}}$/HDS in the single data strobe mode.
5. In 64-bit mode, The "last data register" is the register at address $7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the "last data register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the $\overline{\text{HREQ}}$/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is $\overline{\text{HWR}}$ in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read ($\overline{\text{HRD}}$/HRD) or host write ($\overline{\text{HWR}}$/HWR) in the dual data strobe mode and host data strobe ($\overline{\text{HDS}}$/HDS) in the single data strobe mode.
10. The host request is $\overline{\text{HREQ}}$/HREQ in the single host request mode and $\overline{\text{HRRQ}}$/HRRQ and $\overline{\text{HTRQ}}$/HTRQ in the double host request mode. $\overline{\text{HRRQ}}$/HRRQ is deasserted only when HOTX fifo is empty, $\overline{\text{HTRQ}}$/HTRQ is deasserted only if HORX fifo is full (treat as level Host Request).
11. Compute the value using the expression.

**Figure 2-12** and **Figure 2-13** show HDI16 read signal timing. **Figure 2-14** and **Figure 2-15** show HDI16 write signal timing.
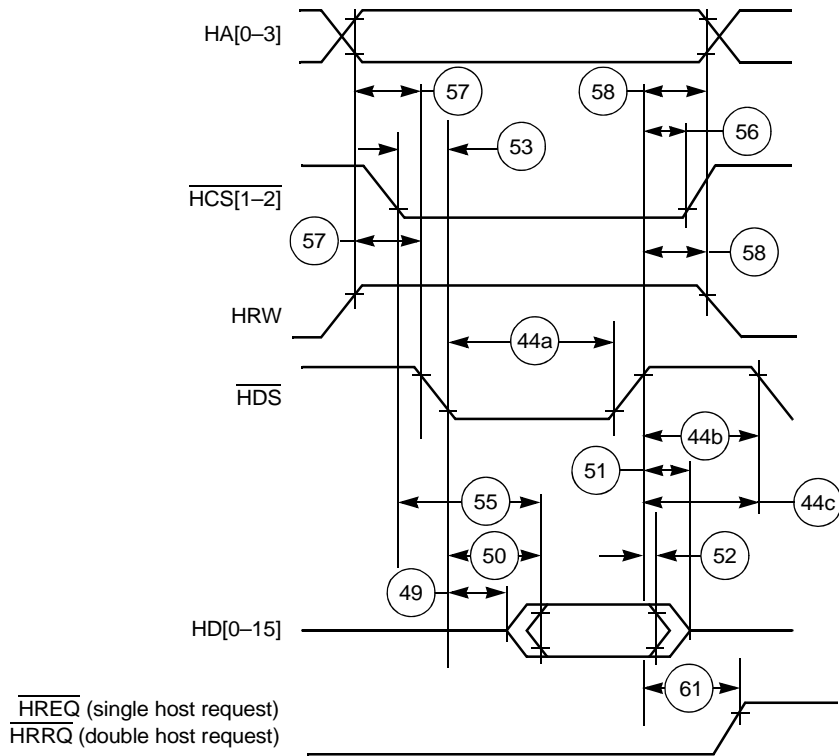
**Figure 2-12.** Read Timing Diagram, Single Data Strobe
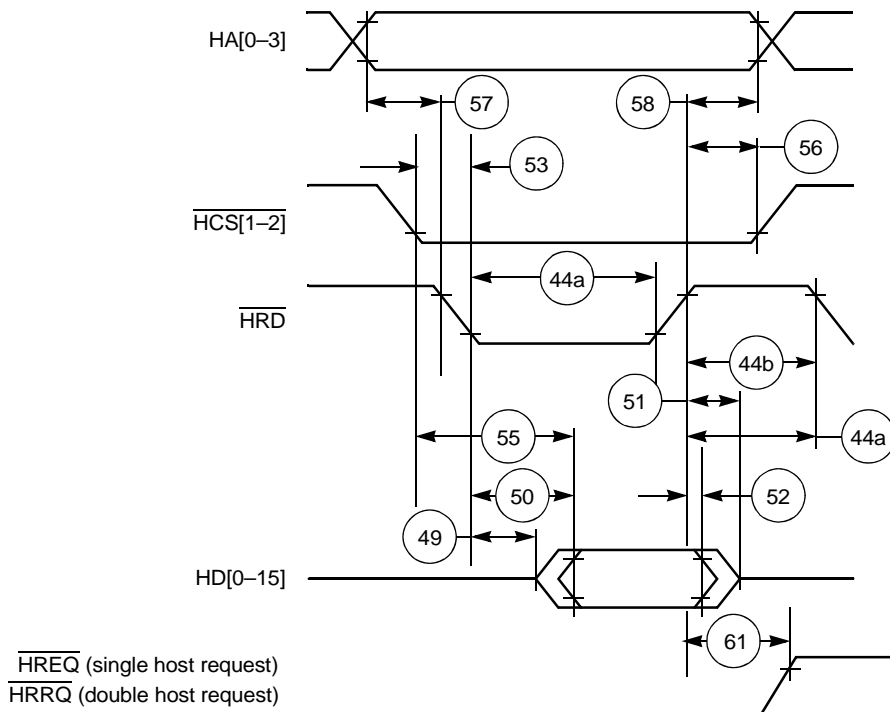


**Figure 2-13.** Read Timing Diagram, Double Data Strobe

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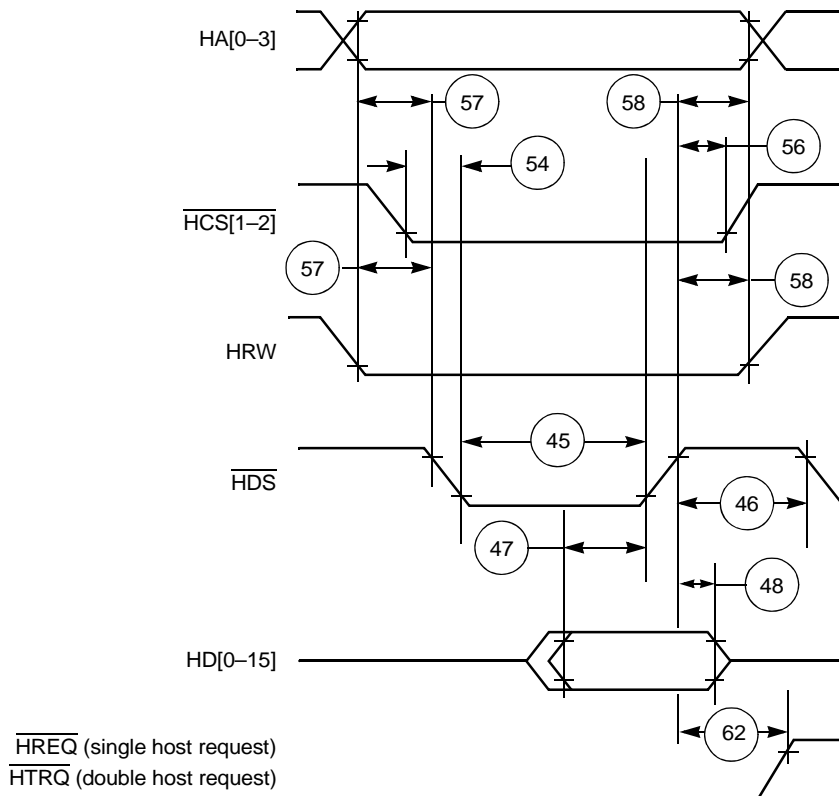
**Figure 2-14.** Write Timing Diagram, Single Data Strobe
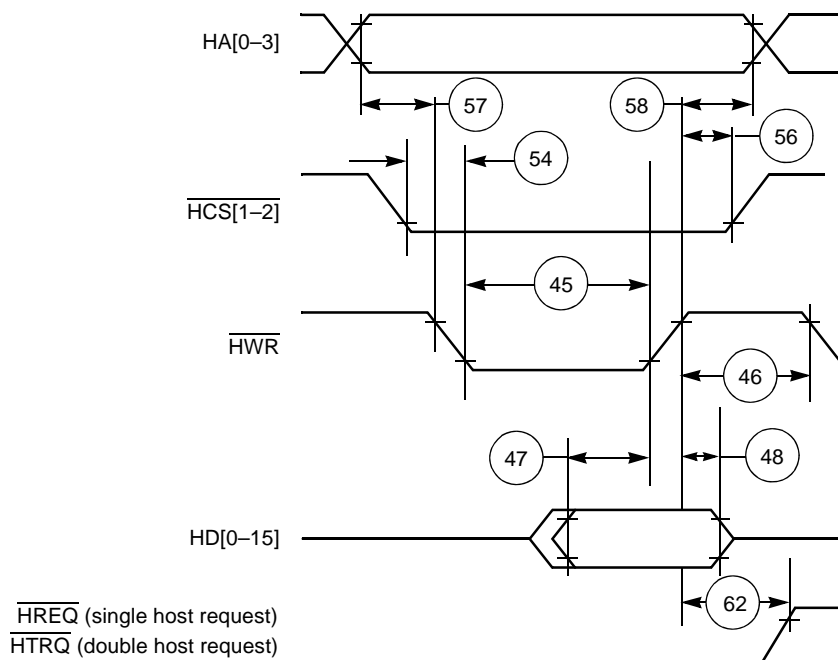


**Figure 2-15.** Write Timing Diagram, Double Data Strobe

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**Figure 2-16** shows Host DMA read timing.



**Figure 2-16.** Host DMA Read Timing Diagram, HPCR[OAD] = 0

**Figure 2-17** shows Host DMA write timing.



**Figure 2-17.** Host DMA Write Timing Diagram, HPCR[OAD] = 0

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# 2.6.7 CPM Timings

**Table 2-20.** CPM Input Characteristics

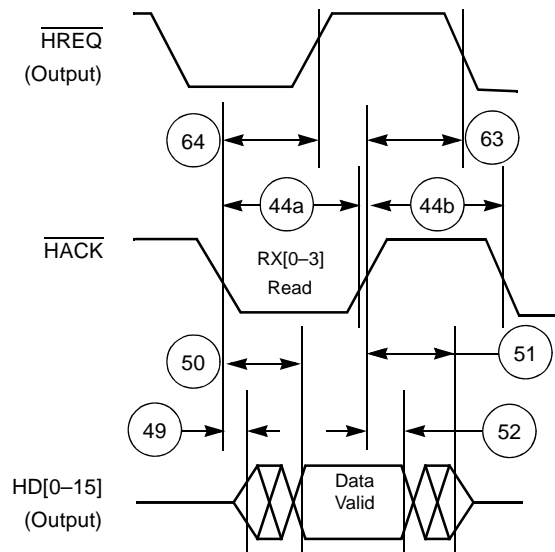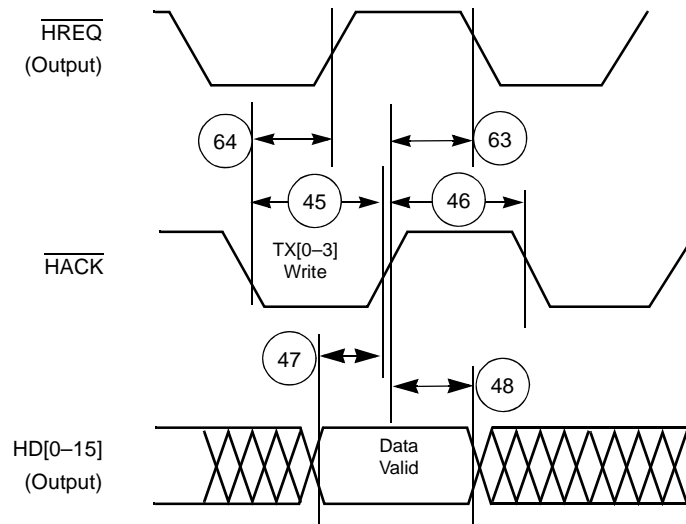| No. | Characteristic | Typical | Unit |
|---|---|---|---|
| 39 | FCC input set-up time before low-to-high clock transition<br>  a. internal clock (BRGxO)<br>  b. external clock (serial clock input) | 10<br>5 | ns<br>ns |
| 17 | FCC input hold time after low-to-high clock transition<br>  a. internal clock (BRGxO)<br>  b. external clock (serial clock input) | 0<br>3 | ns<br>ns |
| 18 | SCC/SMC/SPI/I$^2$C input set-up time before low-to-high clock transition<br>  a. internal clock (BRGxO)<br>  b. external clock (serial clock input) | 20<br>5 | ns<br>ns |
| 19 | SCC/SMC/SPI/I$^2$C input hold time after low-to-high clock transition<br>  a. internal clock (BRGxO)<br>  b. external clock (serial clock input) | 0<br>5 | ns<br>ns |
| 20 | TDM input set-up time before low-to-high serial clock transition | 5 | ns |
| 21 | TDM input hold time after low-to-high serial transition | 5 | ns |
| 22 | PIO/TIMER/DMA input set-up time before low-to-high serial clock transition | 10 | ns |
| 23 | PIO/TIMER/DMA input hold time after low-to-high serial clock transition | 3 | ns |
| **Note:** | FCC, SCC, SMC, SPI, I$^2$C are non-multiplexed serial interface signals. | | |

**Table 2-21.** CPM Output Characteristics

| No. | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| 41 | FCC output delay after low-to-high clock transition<br>  a. internal clock (BRGxO)<br>  b. external clock (serial input clock) | 0<br>2 | 6<br>18 | ns<br>ns |
| 38 | SCC/SMC/SPI/I$^2$C output delay after low-to-high clock transition<br>  a. internal clock (BRGxO)<br>  b. external clock (serial input clock) | 0<br>0 | 20<br>30 | ns<br>ns |
| 40 | TDM output delay after low-to-high serial clock transition | 5 | 15 | ns |
| 42 | PIO/TIMER/DMA output delay after low-to-high serial clock transition | 1 | 14 | ns |
| **Note:** | FCC, SCC, SMC, SPI, I$^2$C are Non-Multiplexed Serial Interface signals. | | | |
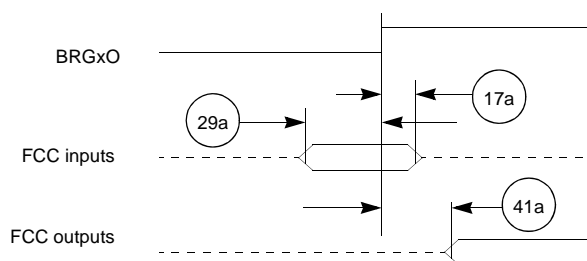


**Figure 2-18.** FCC Internal Clock Diagram
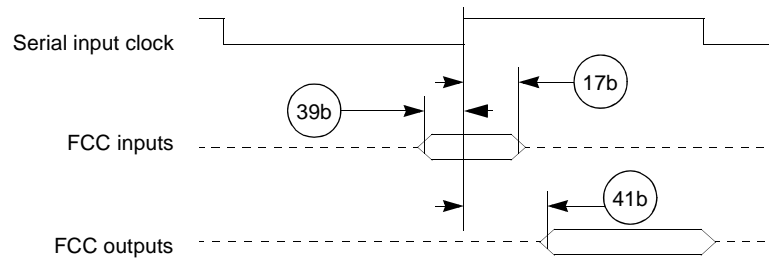
**Figure 2-19.**   FCC External Clock Diagram
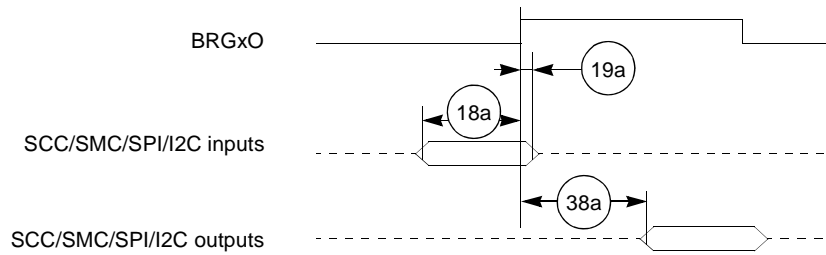


**Figure 2-20.**   SCC/SMC/SPI/I$^2$C Internal Clock Diagram
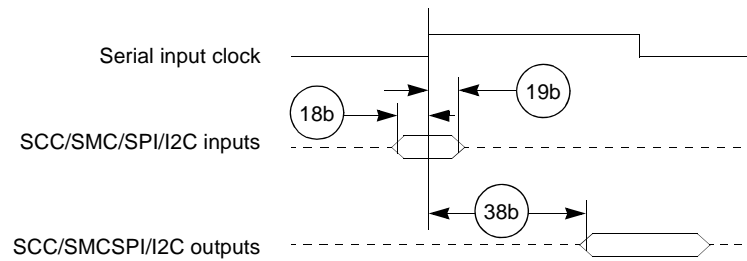


**Figure 2-21.**   SCC/SMC/SPI/I$^2$C External Clock Diagram
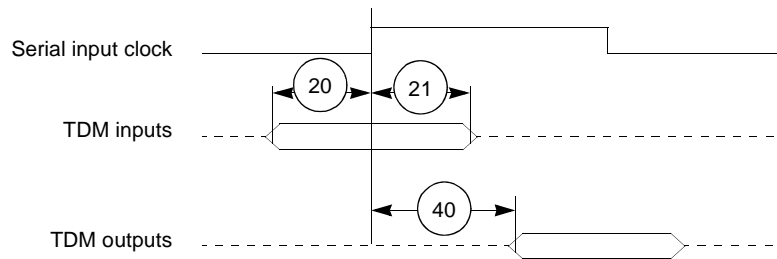


**Figure 2-22.**   TDM Signal Diagram

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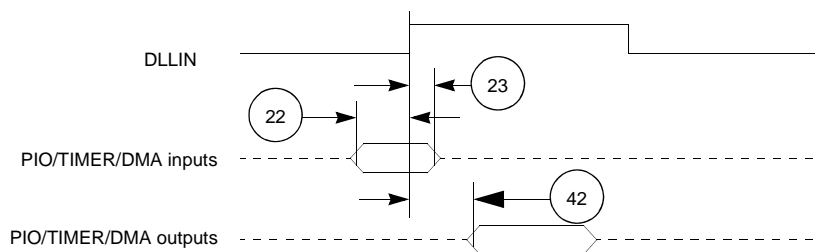
**Figure 2-23.** PIO, Timer, and DMA Signal Diagram

**Note:** The timing values refer to minimum system timing requirements. Actual implementation requires conformance to the specific protocol requirements. Refer to **Chapter 1** to identify the specific input and output signals associated with the referenced internal controllers and supported communication protocols. For example, FCC1 supports ATM/Utopia operation in slave mode, multi-PHY master direct polling mode, and multi-PHY master multiplexed polling mode and each of these modes supports its own set of signals; the direction (input or output) of some of the shared signal names depends on the selected mode.

## 2.6.8  JTAG Signals

**Table 2-22.**  JTAG Timing

| No. | Characteristics | All frequencies | | Unit |
| --- | --- | --- | --- | --- |
| | | Min | Max | |
| 500 | TCK frequency of operation | 0.0 | 40.0 | MHz |
| 501 | TCK cycle time | 25.0 | — | ns |
| 502 | TCK clock pulse width measured at 1.6 V | 12.5 | — | ns |
| 503 | TCK rise and fall times | 0.0 | 3.0 | ns |
| 508 | TMS, TDI data set-up time | 6.0 | — | ns |
| 509 | TMS, TDI data hold time | 3.0 | — | ns |
| 510 | TCK low to TDO data valid | 0.0 | 15.0 | ns |
| 511 | TCK low to TDO high impedance | 0.0 | 20.0 | ns |
| 512 | $\overline{\text{TRST}}$ assert time | 100.0 | — | ns |
| 513 | $\overline{\text{TRST}}$ set-up time to TCK low | 40.0 | — | ns |
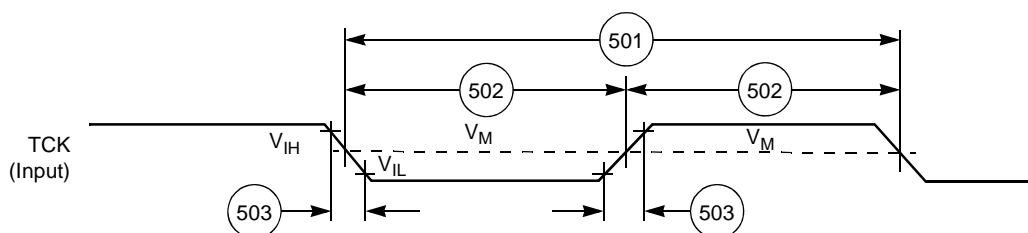


**Figure 2-24.**  Test Clock Input Timing Diagram

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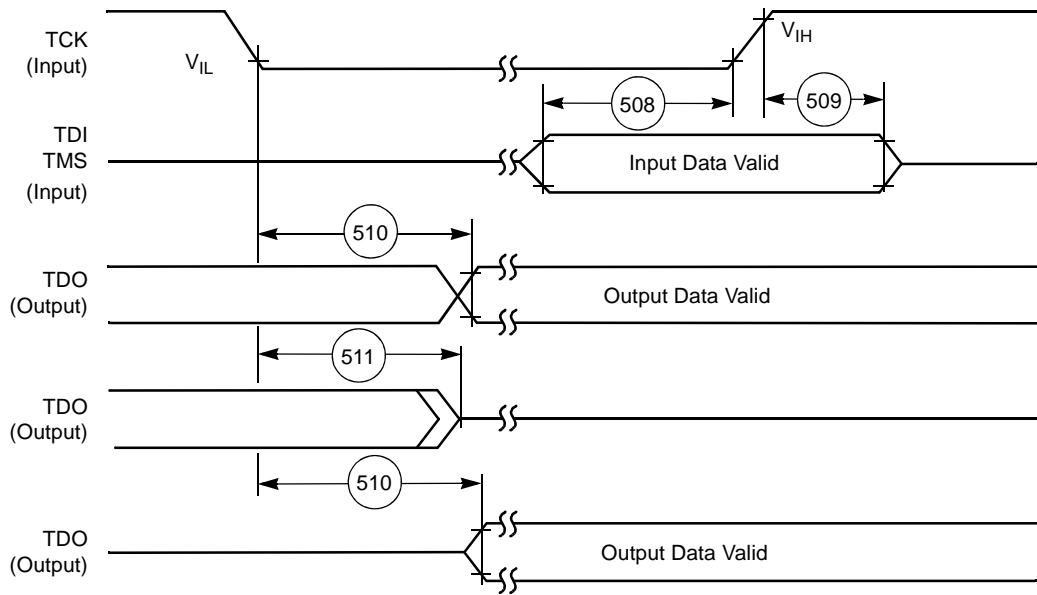
**Figure 2-25.** Test Access Port Timing Diagram
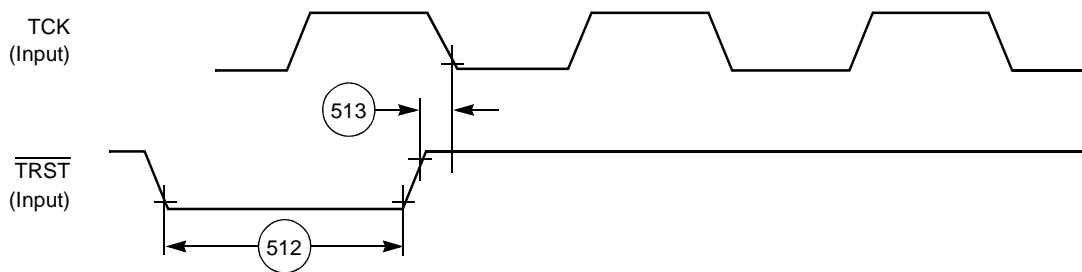


**Figure 2-26.** $\overline{\text{TRST}}$ Timing Diagram

# Packaging 3

This chapter provides information about the MSC8103 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC8103 is available in a 332-pin lidded flip chip-plastic ball grid array (FC-PBGA).

## 3.1  FC-PBGA Package Description

**Figure 3-1** and **Figure 3-2** show top and bottom views of the FC-PBGA package, including pinouts. **Table 3-1** lists the MSC8103 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

**Note:**    The package description in this chapter applies to packages with lead-bearing and lead-free spheres.

Top View
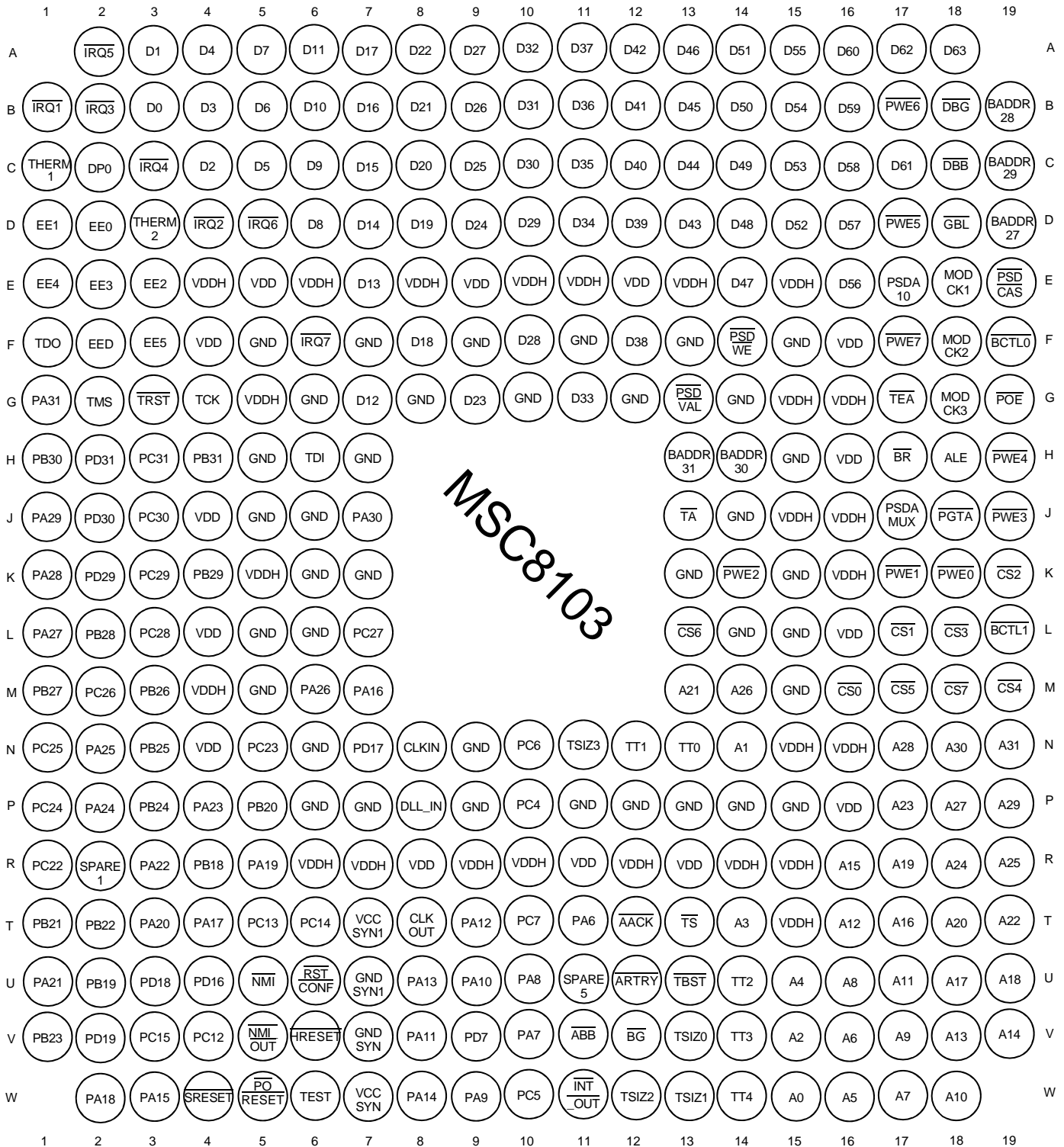


Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

**Figure 3-1.** MSC8103 Flip Chip Plastic Ball Grid Array (FC-PBGA), Top View

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Bottom View



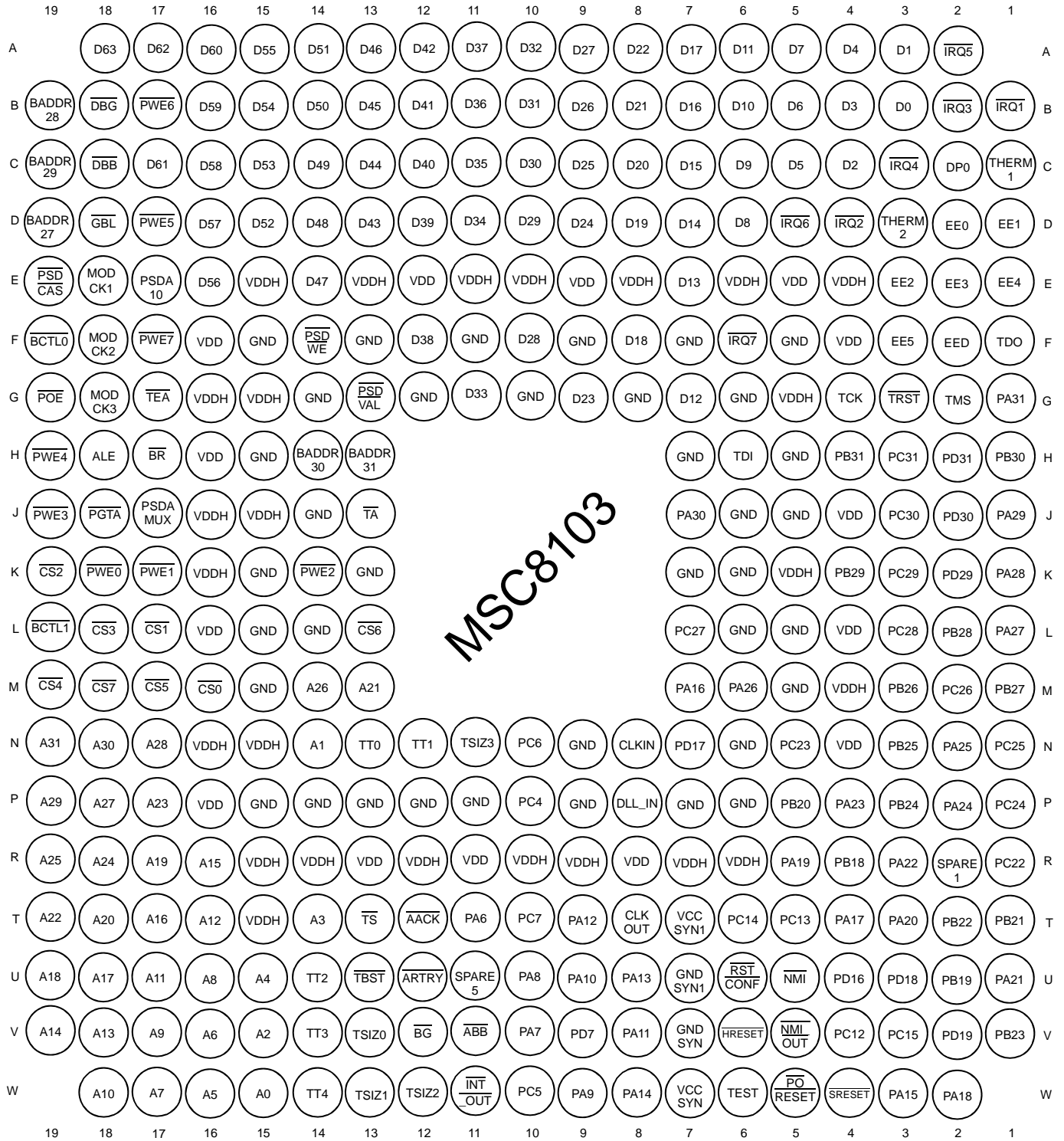| | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | D63 | D62 | D60 | D55 | D51 | D46 | D42 | D37 | D32 | D27 | D22 | D17 | D11 | D7 | D4 | D1 | IRQ5 | | A |
| B | BADDR28 | DBG | PWE6 | D59 | D54 | D50 | D45 | D41 | D36 | D31 | D26 | D21 | D16 | D10 | D6 | D3 | D0 | IRQ3 | IRQ1 | B |
| C | BADDR29 | DBB | D61 | D58 | D53 | D49 | D44 | D40 | D35 | D30 | D25 | D20 | D15 | D9 | D5 | D2 | IRQ4 | DP0 | THERM1 | C |
| D | BADDR27 | GBL | PWE5 | D57 | D52 | D48 | D43 | D39 | D34 | D29 | D24 | D19 | D14 | D8 | IRQ6 | IRQ2 | THERM2 | EE0 | EE1 | D |
| E | PSD/CAS | MODCK1 | PSDA10 | D56 | VDDH | D47 | VDDH | VDD | VDDH | VDDH | VDD | VDDH | D13 | VDDH | VDD | VDDH | EE2 | EE3 | EE4 | E |
| F | BCTL0 | MODCK2 | PWE7 | VDD | GND | PSD/WE | GND | D38 | GND | D28 | GND | D18 | GND | IRQ7 | GND | VDD | EE5 | EED | TDO | F |
| G | POE | MODCK3 | TEA | VDDH | VDDH | GND | PSD/VAL | GND | D33 | GND | D23 | GND | D12 | GND | VDDH | TCK | TRST | TMS | PA31 | G |
| H | PWE4 | ALE | BR | VDD | GND | BADDR30 | BADDR31 | | | | | GND | TDI | GND | PB31 | PC31 | PD31 | PB30 | | H |
| J | PWE3 | PGTA | PSDAMUX | VDDH | VDDH | GND | TA | | | | | PA30 | GND | GND | VDD | PC30 | PD30 | PA29 | | J |
| K | CS2 | PWE0 | PWE1 | VDDH | GND | PWE2 | GND | | | | | GND | GND | VDDH | PB29 | PC29 | PD29 | PA28 | | K |
| L | BCTL1 | CS3 | CS1 | VDD | GND | GND | CS6 | | | | | PC27 | GND | GND | VDD | PC28 | PB28 | PA27 | | L |
| M | CS4 | CS7 | CS5 | CS0 | GND | A26 | A21 | | | | | PA16 | PA26 | GND | VDDH | PB26 | PC26 | PB27 | | M |
| N | A31 | A30 | A28 | VDDH | VDDH | A1 | TT0 | TT1 | TSIZ3 | PC6 | GND | CLKIN | PD17 | GND | PC23 | VDD | PB25 | PA25 | PC25 | N |
| P | A29 | A27 | A23 | VDD | GND | GND | GND | GND | GND | PC4 | GND | DLL_IN | GND | GND | PB20 | PA23 | PB24 | PA24 | PC24 | P |
| R | A25 | A24 | A19 | A15 | VDDH | VDDH | VDD | VDDH | VDD | VDDH | VDDH | VDD | VDDH | VDDH | PA19 | PB18 | PA22 | SPARE1 | PC22 | R |
| T | A22 | A20 | A16 | A12 | VDDH | A3 | TS | AACK | PA6 | PC7 | PA12 | CLKOUT | VCCSYN1 | PC14 | PC13 | PA17 | PA20 | PB22 | PB21 | T |
| U | A18 | A17 | A11 | A8 | A4 | TT2 | TBST | ARTRY | SPARE5 | PA8 | PA10 | PA13 | GNDSYN1 | RST/CONF | NMI | PD16 | PD18 | PB19 | PA21 | U |
| V | A14 | A13 | A9 | A6 | A2 | TT3 | TSIZ0 | BG | ABB | PA7 | PD7 | PA11 | GNDSYN | HRESET | NMIOUT | PC12 | PC15 | PD19 | PB23 | V |
| W | | A10 | A7 | A5 | A0 | TT4 | TSIZ1 | TSIZ2 | INT/OUT | PC5 | PA9 | PA14 | VCCSYN | TEST | PO/RESET | SRESET | PA15 | PA18 | | W |
| | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

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**Note**: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

**Figure 3-2.**  MSC8103 Flip Chip Plastic Ball Grid Array (FC-PBGA), Bottom Vie

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**Table 3-1.** MSC8103 Signal Listing By Name

| Signal Name | Number |
|:---:|:---:|
| A0 | W15 |
| A1 | N14 |
| A2 | V15 |
| A3 | T14 |
| A4 | U15 |
| A5 | W16 |
| A6 | V16 |
| A7 | W17 |
| A8 | U16 |
| A9 | V17 |
| A10 | W18 |
| A11 | U17 |
| A12 | T16 |
| A13 | V18 |
| A14 | V19 |
| A15 | R16 |
| A16 | T17 |
| A17 | U18 |
| A18 | U19 |
| A19 | R17 |
| A20 | T18 |
| A21 | M13 |
| A22 | T19 |
| A23 | P17 |
| A24 | R18 |
| A25 | R19 |
| A26 | M14 |
| A27 | P18 |
| A28 | N17 |
| A29 | P19 |
| A30 | N18 |
| A31 | N19 |
| $\overline{\text{AACK}}$ | T12 |
| $\overline{\text{ABB}}$ | V11 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| ALE | H18 |
| $\overline{\text{ARTRY}}$ | U12 |
| BADDR27 | D19 |
| BADDR28 | B19 |
| BADDR29 | C19 |
| BADDR30 | H14 |
| BADDR31 | H13 |
| $\overline{\text{BCTL0}}$ | F19 |
| $\overline{\text{BCTL1}}$ | L19 |
| BG | V12 |
| BNKSEL0 | E18 |
| BNKSEL1 | F18 |
| BNKSEL2 | G18 |
| $\overline{\text{BR}}$ | H17 |
| BRG1O | H3 |
| BRG1O | V2 |
| BRG2O | J3 |
| BRG2O | N7 |
| BRG3O | K3 |
| BRG4O | L3 |
| BRG5O | L7 |
| BRG6O | M2 |
| BRG7O | N1 |
| BRG8O | P1 |
| BTM0 | E1 |
| BTM1 | F3 |
| $\overline{\text{CD}}$ for FCC1 | N10 |
| $\overline{\text{CD}}$ for FCC2 | P10 |
| $\overline{\text{CD}}$/RENA for SCC1 | T6 |
| $\overline{\text{CD}}$/RENA for SCC2 | V4 |
| CLK1 | H3 |
| CLK2 | J3 |
| CLK3 | K3 |
| CLK4 | L3 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|:---:|:---:|
| CLK5 | L7 |
| CLK6 | M2 |
| CLK7 | N1 |
| CLK8 | P1 |
| CLK9 | N5 |
| CLK10 | R1 |
| CLKIN | N8 |
| CLKOUT | T8 |
| COL for FCC1 | G1 |
| COL for FCC2 | M1 |
| CRS for FCC1 | J7 |
| CRS for FCC2 | M3 |
| $\overline{\text{CS0}}$ | M16 |
| $\overline{\text{CS1}}$ | L17 |
| $\overline{\text{CS2}}$ | K19 |
| $\overline{\text{CS3}}$ | L18 |
| $\overline{\text{CS4}}$ | M19 |
| $\overline{\text{CS5}}$ | M17 |
| $\overline{\text{CS6}}$ | L13 |
| $\overline{\text{CS7}}$ | M18 |
| $\overline{\text{CTS}}$ for FCC1 | T10 |
| $\overline{\text{CTS}}$ for FCC2 | W10 |
| $\overline{\text{CTS}}$/CLSN for SCC1 | K3 |
| $\overline{\text{CTS}}$/CLSN for SCC1 | V3 |
| $\overline{\text{CTS}}$/CLSN for SCC2 | L3 |
| $\overline{\text{CTS}}$/CLSN for SCC2 | T5 |
| D0 | B3 |
| D1 | A3 |
| D2 | C4 |
| D3 | B4 |
| D4 | A4 |
| D5 | C5 |
| D6 | B5 |
| D7 | A5 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|:---:|:---:|
| D8 | D6 |
| D9 | C6 |
| D10 | B6 |
| D11 | A6 |
| D12 | G7 |
| D13 | E7 |
| D14 | D7 |
| D15 | C7 |
| D16 | B7 |
| D17 | A7 |
| D18 | F8 |
| D19 | D8 |
| D20 | C8 |
| D21 | B8 |
| D22 | A8 |
| D23 | G9 |
| D24 | D9 |
| D25 | C9 |
| D26 | B9 |
| D27 | A9 |
| D28 | F10 |
| D29 | D10 |
| D30 | C10 |
| D31 | B10 |
| D32 | A10 |
| D33 | G11 |
| D34 | D11 |
| D35 | C11 |
| D36 | B11 |
| D37 | A11 |
| D38 | F12 |
| D39 | D12 |
| D40 | C12 |
| D41 | B12 |

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**Table 3-1.**    MSC8103 Signal Listing By Name  (Continued)

| Signal Name | Number |
|:---:|:---:|
| D42 | A12 |
| D43 | D13 |
| D44 | C13 |
| D45 | B13 |
| D46 | A13 |
| D47 | E14 |
| D48 | D14 |
| D49 | C14 |
| D50 | B14 |
| D51 | A14 |
| D52 | D15 |
| D53 | C15 |
| D54 | B15 |
| D55 | A15 |
| D56 | E16 |
| D57 | D16 |
| D58 | C16 |
| D59 | B16 |
| D60 | A16 |
| D61 | C17 |
| D62 | A17 |
| D63 | A18 |
| $\overline{\text{DACK1}}$ | N5 |
| $\overline{\text{DACK2}}$ | N1 |
| $\overline{\text{DACK3}}$ | D5 |
| $\overline{\text{DACK4}}$ | F6 |
| $\overline{\text{DBB}}$ | C18 |
| $\overline{\text{DBG}}$ | B18 |
| DBREQ | D2 |
| DLLIN | P8 |
| DP0 | C2 |
| DP1 | B1 |
| DP2 | D4 |
| DP3 | B2 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|:---:|:---:|
| DP4 | C3 |
| DP5 | A2 |
| DP6 | D5 |
| DP7 | F6 |
| $\overline{\text{DRACK1}}$/$\overline{\text{DONE1}}$ | H2 |
| $\overline{\text{DRACK2}}$/$\overline{\text{DONE2}}$ | J2 |
| DREQ1 | R1 |
| DREQ2 | P1 |
| DREQ3 | C3 |
| DREQ4 | A2 |
| EE0 | D2 |
| EE1 | D1 |
| EE2 | E3 |
| EE3 | E2 |
| EE4 | E1 |
| EE5 | F3 |
| EED | F2 |
| $\overline{\text{EXT\_BG2}}$ | B1 |
| $\overline{\text{EXT\_BG3}}$ | C3 |
| $\overline{\text{EXT\_BR2}}$ | C2 |
| $\overline{\text{EXT\_BR3}}$ | B2 |
| $\overline{\text{EXT\_DBG2}}$ | D4 |
| $\overline{\text{EXT\_DBG3}}$ | A2 |
| EXT1 | H3 |
| EXT2 | N5 |
| $\overline{\text{GBL}}$ | D18 |
| GND | F11 |
| GND | F13 |
| GND | F15 |
| GND | F5 |
| GND | F7 |
| GND | F9 |
| GND | G10 |
| GND | G12 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| GND | G14 |
| GND | G6 |
| GND | G8 |
| GND | H15 |
| GND | H5 |
| GND | H7 |
| GND | J14 |
| GND | J5 |
| GND | J6 |
| GND | K13 |
| GND | K15 |
| GND | K6 |
| GND | K7 |
| GND | L14 |
| GND | L15 |
| GND | L5 |
| GND | L6 |
| GND | M15 |
| GND | M5 |
| GND | N6 |
| GND | N9 |
| GND | P11 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | P15 |
| GND | P6 |
| GND | P7 |
| GND | P9 |
| GND$_{SYN}$ | V7 |
| GND$_{SYN1}$ | U7 |
| H8BIT | B16 |
| HA0 | D14 |
| HA1 | C14 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| HA2 | B14 |
| HA3 | A14 |
| $\overline{\text{HACK}}$/HACK | E16 |
| $\overline{\text{HCS1}}$/HCS1 | D15 |
| $\overline{\text{HCS2}}$/HCS2 | A16 |
| HD0 | A10 |
| HD1 | G11 |
| HD2 | D11 |
| HD3 | C11 |
| HD4 | B11 |
| HD5 | A11 |
| HD6 | F12 |
| HD7 | D12 |
| HD8 | C12 |
| HD9 | B12 |
| HD10 | A12 |
| HD11 | D13 |
| HD12 | C13 |
| HD13 | B13 |
| HD14 | A13 |
| HD15 | E14 |
| HDDS | C16 |
| $\overline{\text{HDS}}$/HDS | B15 |
| HDSP | D16 |
| HPE | D1 |
| $\overline{\text{HRD}}$/HRD | C15 |
| $\overline{\text{HREQ}}$/HREQ | A15 |
| HRESET | V6 |
| $\overline{\text{HRRQ}}$/HRRQ | E16 |
| HRW | C15 |
| $\overline{\text{HTRQ}}$/HTRQ | A15 |
| $\overline{\text{HWR}}$/HWR | B15 |
| $\overline{\text{INT\_OUT}}$ | W11 |
| $\overline{\text{IRQ1}}$ | B1 |

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**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| $\overline{\text{IRQ1}}$ | D18 |
| $\overline{\text{IRQ2}}$ | C19 |
| $\overline{\text{IRQ2}}$ | D4 |
| $\overline{\text{IRQ2}}$ | V11 |
| $\overline{\text{IRQ3}}$ | B2 |
| $\overline{\text{IRQ3}}$ | C18 |
| $\overline{\text{IRQ3}}$ | H14 |
| $\overline{\text{IRQ4}}$ | C3 |
| $\overline{\text{IRQ5}}$ | A2 |
| $\overline{\text{IRQ5}}$ | H13 |
| $\overline{\text{IRQ6}}$ | D5 |
| $\overline{\text{IRQ7}}$ | F6 |
| $\overline{\text{IRQ7}}$ | W11 |
| L1RSYNC for SI1 TDMA1 | T11 |
| L1RSYNC for SI2 TDMB2 | K4 |
| L1RSYNC for SI2 TDMC2 | P3 |
| L1RSYNC for SI2 TDMD2 | P5 |
| L1RXD for SI1 TDMA1 Serial | U10 |
| L1RXD for SI2 TDMB2 | H1 |
| L1RXD for SI2 TDMC2 | M3 |
| L1RXD for SI2 TDMD2 | T2 |
| L1RXD0 for SI1 TDMA1 Nibble | U10 |
| L1RXD1 for SI1 TDMA1 Nibble | T2 |
| L1RXD2 for SI1 TDMA1 Nibble | V1 |
| L1RXD3 for SI1 TDMA1 Nibble | P3 |
| L1TSYNC for SI1 TDMA1 | V10 |
| L1TSYNC for SI2 TDMB2 | L2 |
| L1TSYNC for SI2 TDMC2 | N3 |
| L1TSYNC for SI2 TDMD2 | T1 |
| L1TXD for SI1 TDMA1 Serial | W9 |
| L1TXD for SI2 TDMB2 | H4 |
| L1TXD for SI2 TDMC2 | M1 |
| L1TXD for SI2 TDMD2 | V1 |
| L1TXD0 for SI1 TDMA1 Nibble | W9 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| L1TXD1 for SI1 TDMA1 Nibble | P5 |
| L1TXD2 for SI1 TDMA1 Nibble | T1 |
| L1TXD3 for SI1 TDMA1 Nibble | N3 |
| LIST1 for SI1 | R1 |
| LIST1 for SI2 | T10 |
| LIST2 for SI1 | T6 |
| LIST2 for SI2 | N10 |
| LIST3 for SI1 | V4 |
| LIST3 for SI2 | W10 |
| LIST4 for SI1 | T5 |
| LIST4 for SI2 | P10 |
| MODCK1 | E18 |
| MODCK2 | F18 |
| MODCK3 | G18 |
| MSNUM0 | N2 |
| MSNUM1 | P2 |
| MSNUM2 | U8 |
| MSNUM3 | T9 |
| MSNUM4 | V8 |
| MSNUM5 | U9 |
| $\overline{\text{NMI}}$ | U5 |
| $\overline{\text{NMI\_OUT}}$ | V5 |
| PA6 | T11 |
| PA7 | V10 |
| PA8 | U10 |
| PA9 | W9 |
| PA10 | U9 |
| PA11 | V8 |
| PA12 | T9 |
| PA13 | U8 |
| PA14 | W8 |
| PA15 | W3 |
| PA16 | M7 |
| PA17 | T4 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.**    MSC8103 Signal Listing By Name  (Continued)

| Signal Name | Number |
|:---:|:---:|
| PA18 | W2 |
| PA19 | R5 |
| PA20 | T3 |
| PA21 | U1 |
| PA22 | R3 |
| PA23 | P4 |
| PA24 | P2 |
| PA25 | N2 |
| PA26 | M6 |
| PA27 | L1 |
| PA28 | K1 |
| PA29 | J1 |
| PA30 | J7 |
| PA31 | G1 |
| PB18 | R4 |
| PB19 | U2 |
| PB20 | P5 |
| PB21 | T1 |
| PB22 | T2 |
| PB23 | V1 |
| PB24 | P3 |
| PB25 | N3 |
| PB26 | M3 |
| PB27 | M1 |
| PB28 | L2 |
| PB29 | K4 |
| PB30 | H1 |
| PB31 | H4 |
| $\overline{PBS0}$ | K18 |
| $\overline{PBS1}$ | K17 |
| $\overline{PBS2}$ | K14 |
| $\overline{PBS3}$ | J19 |
| $\overline{PBS4}$ | H19 |
| $\overline{PBS5}$ | D17 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.**    MSC8103 Signal Listing By Name  (Continued)

| Signal Name | Number |
|:---:|:---:|
| $\overline{\text{PBS6}}$ | B17 |
| $\overline{\text{PBS7}}$ | F17 |
| PC4 | P10 |
| PC5 | W10 |
| PC6 | N10 |
| PC7 | T10 |
| PC12 | V4 |
| PC13 | T5 |
| PC14 | T6 |
| PC15 | V3 |
| PC22 | R1 |
| PC23 | N5 |
| PC24 | P1 |
| PC25 | N1 |
| PC26 | M2 |
| PC27 | L7 |
| PC28 | L3 |
| PC29 | K3 |
| PC30 | J3 |
| PC31 | H3 |
| PD7 | V9 |
| PD16 | U4 |
| PD17 | N7 |
| PD18 | U3 |
| PD19 | V2 |
| PD29 | K2 |
| PD30 | J2 |
| PD31 | H2 |
| PGPL0 | E17 |
| PGPL1 | F14 |
| PGPL2 | G19 |
| PGPL3 | E19 |
| PGPL4 | J18 |
| PGPL5 | J17 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| $\overline{\text{PGTA}}$ | J18 |
| $\overline{\text{POE}}$ | G19 |
| $\overline{\text{PORESET}}$ | W5 |
| $\overline{\text{PPBS}}$ | J18 |
| PSDA10 | E17 |
| PSDAMUX | J17 |
| $\overline{\text{PSDCAS}}$ | E19 |
| $\overline{\text{PSDDQM0}}$ | K18 |
| $\overline{\text{PSDDQM1}}$ | K17 |
| $\overline{\text{PSDDQM2}}$ | K14 |
| $\overline{\text{PSDDQM3}}$ | J19 |
| $\overline{\text{PSDDQM4}}$ | H19 |
| $\overline{\text{PSDDQM5}}$ | D17 |
| $\overline{\text{PSDDQM6}}$ | B17 |
| $\overline{\text{PSDDQM7}}$ | F17 |
| $\overline{\text{PSDRAS}}$ | G19 |
| $\overline{\text{PSDVAL}}$ | G13 |
| $\overline{\text{PSDWE}}$ | F14 |
| PUPMWAIT | J18 |
| $\overline{\text{PWE0}}$ | K18 |
| $\overline{\text{PWE1}}$ | K17 |
| $\overline{\text{PWE2}}$ | K14 |
| $\overline{\text{PWE3}}$ | J19 |
| $\overline{\text{PWE4}}$ | H19 |
| $\overline{\text{PWE5}}$ | D17 |
| $\overline{\text{PWE6}}$ | B17 |
| $\overline{\text{PWE7}}$ | F17 |
| Reserved | A17 |
| Reserved | A18 |
| Reserved | C2 |
| Reserved | C17 |
| Reserved | C19 |
| Reserved | H14 |
| Reserved | H13 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name  (Continued)

| Signal Name | Number |
|---|---|
| $\overline{\text{RSTCONF}}$ | U6 |
| $\overline{\text{RTS}}$ for FCC1 | J7 |
| $\overline{\text{RTS}}$ for FCC2 | L2 |
| $\overline{\text{RTS}}$/TENA for SCC1 | K2 |
| $\overline{\text{RTS}}$/TENA for SCC2 | L2 |
| RX_DV for FCC1 | L1 |
| RX_DV for FCC2 | H1 |
| RX_ER for FCC1 | M6 |
| RX_ER for FCC2 | L2 |
| RXADDR0 for FCC1 UTOPIA 8 | T6 |
| RXADDR1 for FCC1 UTOPIA 8 | V4 |
| RXADDR2 for FCC1 UTOPIA 8 | N10 |
| RXADDR2/RXCLAV1 for FCC1 UTOPIA 8 | N10 |
| RXADDR3 for FCC1 UTOPIA 8 | K2 |
| RXADDR4 for FCC1 UTOPIA 8 | U3 |
| RXCLAV for FCC1 UTOPIA 8 | M6 |
| RXCLAV0 for FCC1 UTOPIA 8 | M6 |
| RXCLAV2 for FCC1 UTOPIA 8 | K2 |
| RXCLAV3 for FCC1 UTOPIA 8 | V4 |
| RXD for FCC1 transparent/HDLC serial | T4 |
| RXD for FCC2 transparent/HDLC serial | T1 |
| RXD for SCC1 | H2 |
| RXD for SCC2 | H4 |
| RXD0 for FCC1 MII/HDLC nibble | T4 |
| RXD0 for FCC1 UTOPIA 8 | U9 |
| RXD0 for FCC2 MII/HDLC nibble | T1 |
| RXD1 for FCC1 MII/HDLC nibble | M7 |
| RXD1 for FCC1 UTOPIA 8 | V8 |
| RXD1 for FCC2 MII/HDLC nibble | P5 |
| RXD2 for FCC1 MII/HDLC nibble | W3 |
| RXD2 for FCC1 UTOPIA 8 | T9 |
| RXD2 for FCC2 MII/HDLC nibble | U2 |
| RXD3 for FCC1 MII/HDLC nibble | W8 |
| RXD3 for FCC1 UTOPIA 8 | U8 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| RXD3 for FCC2 MII/HDLC nibble | R4 |
| RXD4 for FCC1 UTOPIA 8 | W8 |
| RXD5 for FCC1 UTOPIA 8 | W3 |
| RXD6 for FCC1 UTOPIA 8 | M7 |
| RXD7 for FCC1 UTOPIA 8 | T4 |
| $\overline{\text{RXENB}}$ for FCC1 | K1 |
| RXPRTY for FCC1 UTOPIA 8 | N7 |
| RXSOC for FCC1 | L1 |
| SCL | R4 |
| SDA | U2 |
| SMRXD for SMC1 | P10 |
| SMRXD for SMC2 | U10 |
| $\overline{\text{SMSYN}}$ for SMC1 | V9 |
| $\overline{\text{SMSYN}}$ for SMC2 | V10 |
| SMTXD for SMC1 | W10 |
| SMTXD for SMC2 | W9 |
| SMTXD for SMC2 | V3 |
| SPARE1 | R2 |
| SPARE5 | U11 |
| SPICLK | U3 |
| SPIMISO | U4 |
| SPIMOSI | N7 |
| $\overline{\text{SPISEL}}$ | V2 |
| $\overline{\text{SRESET}}$ | W4 |
| $\overline{\text{TA}}$ | J13 |
| $\overline{\text{TBST}}$ | U13 |
| TC0 | E18 |
| TC1 | F18 |
| TC2 | G18 |
| TCK | G4 |
| TDI | H6 |
| TDO | F1 |
| $\overline{\text{TEA}}$ | G17 |
| TEST | W6 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|:---:|:---:|
| $\overline{\text{TGATE1}}$ | H3 |
| $\overline{\text{TGATE2}}$ | L7 |
| THERM1 | C1 |
| THERM2 | D3 |
| TIN1/$\overline{\text{TOUT2}}$ | L3 |
| TIN2 | K3 |
| TIN3/$\overline{\text{TOUT4}}$ | P1 |
| TIN4 | N1 |
| TMCLK | M2 |
| TMS | G2 |
| $\overline{\text{TOUT1}}$ | J3 |
| $\overline{\text{TOUT3}}$ | M2 |
| $\overline{\text{TRST}}$ | G3 |
| $\overline{\text{TS}}$ | T13 |
| TSIZ0 | V13 |
| TSIZ1 | W13 |
| TSIZ2 | W12 |
| TSIZ3 | N11 |
| TT0 | N13 |
| TT1 | N12 |
| TT2 | U14 |
| TT3 | V14 |
| TT4 | W14 |
| TX_EN for FCC1 MII | K1 |
| TX_EN for FCC2 MII | K4 |
| TX_ER for FCC1 MII | J1 |
| TX_ER for FCC2 MII | H4 |
| TXADDR0 for FCC1 UTOPIA 8 | V3 |
| TXADDR1 for FCC1 UTOPIA 8 | T5 |
| TXADDR2 for FCC1 UTOPIA 8 | T10 |
| TXADDR2 for FCC1 UTOPIA 8 | T10 |
| TXADDR3 for FCC1 UTOPIA 8 | V9 |
| TXADDR4 for FCC1 UTOPIA 8 | V2 |
| TXCLAV for FCC1 UTOPIA 8 | J7 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name  (Continued)

| Signal Name | Number |
|---|---|
| TXCLAV0 for FCC1 UTOPIA 8 | J7 |
| TXCLAV1 for FCC1 UTOPIA 8 | T10 |
| TXCLAV2 for FCC1 UTOPIA 8 | V9 |
| TXCLAV3 for FCC1 UTOPIA 8 | V2 |
| TXD for FCC1 transparent/HDLC serial | W2 |
| TXD for FCC2 transparent/HDLC serial | T2 |
| TXD for SCC1 | J2 |
| TXD for SCC2 | H1 |
| TXD0 for FCC1 MII/HDLC nibble | W2 |
| TXD0 for FCC1 UTOPIA 8 | N2 |
| TXD0 for FCC2 MII/HDLC nibble | T2 |
| TXD1 for FCC1 MII/HDLC nibble | R5 |
| TXD1 for FCC1 UTOPIA 8 | P2 |
| TXD1 for FCC2 MII/HDLC nibble | V1 |
| TXD2 for FCC1 MII/HDLC nibble | T3 |
| TXD2 for FCC1 UTOPIA 8 | P4 |
| TXD2 for FCC2 MII/HDLC nibble | P3 |
| TXD3 for FCC1 MII/HDLC nibble | U1 |
| TXD3 for FCC1 UTOPIA 8 | R3 |
| TXD3 for FCC2 MII/HDLC nibble | N3 |
| TXD4 for FCC1 UTOPIA 8 | U1 |
| TXD5 for FCC1 UTOPIA 8 | T3 |
| TXD6 for FCC1 UTOPIA 8 | R5 |
| TXD7 for FCC1 UTOPIA 8 | W2 |
| $\overline{\text{TXENB}}$ for FCC1 | G1 |
| TXPRTY for FCC1 UTOPIA 8 | U4 |
| TXSOC for FCC1 | J1 |
| $V_{CCSYN}$ | W7 |
| $V_{CCSYN1}$ | T7 |
| $V_{DD}$ | E12 |
| $V_{DD}$ | E5 |
| $V_{DD}$ | E9 |
| $V_{DD}$ | F16 |
| $V_{DD}$ | F4 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| $V_{DD}$ | H16 |
| $V_{DD}$ | J4 |
| $V_{DD}$ | L16 |
| $V_{DD}$ | L4 |
| $V_{DD}$ | N4 |
| $V_{DD}$ | P16 |
| $V_{DD}$ | R11 |
| $V_{DD}$ | R13 |
| $V_{DD}$ | R8 |
| $V_{DDH}$ | E10 |
| $V_{DDH}$ | E11 |
| $V_{DDH}$ | E13 |
| $V_{DDH}$ | E15 |
| $V_{DDH}$ | E4 |
| $V_{DDH}$ | E6 |
| $V_{DDH}$ | E8 |
| $V_{DDH}$ | G15 |
| $V_{DDH}$ | G16 |
| $V_{DDH}$ | G5 |
| $V_{DDH}$ | J15 |
| $V_{DDH}$ | J16 |
| $V_{DDH}$ | K16 |
| $V_{DDH}$ | K5 |
| $V_{DDH}$ | M4 |
| $V_{DDH}$ | N15 |
| $V_{DDH}$ | N16 |
| $V_{DDH}$ | R10 |
| $V_{DDH}$ | R12 |
| $V_{DDH}$ | R14 |
| $V_{DDH}$ | R15 |
| $V_{DDH}$ | R6 |
| $V_{DDH}$ | R7 |
| $V_{DDH}$ | R9 |
| $V_{DDH}$ | T15 |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-2.** MSC8103 Signal Listing by Pin Designator

| Number | Signal Name |
|--------|-------------|
| A2 | $\overline{IRQ5}$ / DP5 / DREQ4 / $\overline{EXT\_DBG3}$ |
| A3 | D1 |
| A4 | D4 |
| A5 | D7 |
| A6 | D11 |
| A7 | D17 |
| A8 | D22 |
| A9 | D27 |
| A10 | D32 / HD0 |
| A11 | D37 / HD5 |
| A12 | D42 / HD10 |
| A13 | D46 / HD14 |
| A14 | D51 / HA3 |
| A15 | D55 / $\overline{HREQ}$ / $\overline{HTRQ}$ |
| A16 | D60 / $\overline{HCS2}$ |
| A17 | D62 / Reserved |
| A18 | D63 / Reserved |
| B1 | $\overline{IRQ1}$ / DP1 / $\overline{EXT\_BG2}$ |
| B2 | $\overline{IRQ3}$ / DP3 / $\overline{EXT\_BR3}$ |
| B3 | D0 |
| B4 | D3 |
| B5 | D6 |
| B6 | D10 |
| B7 | D16 |
| B8 | D21 |
| B9 | D26 |
| B10 | D31 |
| B11 | D36 / HD4 |
| B12 | D41 / HD9 |
| B13 | D45 / HD13 |
| B14 | D50 / HA2 |
| B15 | D54 / $\overline{HDS}$ / $\overline{HWR}$ |
| B16 | D59 / H8BIT |
| B17 | $\overline{PWE6}$ / $\overline{PSDDQM6}$ / $\overline{PBS6}$ |
| B18 | $\overline{DBG}$ |
| B19 | BADDR28 |
| C1 | THERM1 |
| C2 | Reserved / DP0 / $\overline{EXT\_BR2}$ |
| C3 | $\overline{IRQ4}$ / DP4 / DREQ3 / $\overline{EXT\_BG3}$ |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|--------|-------------|
| C4 | D2 |
| C5 | D5 |
| C6 | D9 |
| C7 | D15 |
| C8 | D20 |
| C9 | D25 |
| C10 | D30 |
| C11 | D35 / HD3 |
| C12 | D40 / HD8 |
| C13 | D44 / HD12 |
| C14 | D49 / HA1 |
| C15 | D53 / HRW / $\overline{\text{HRD}}$ |
| C16 | D58 / HDDS |
| C17 | D61 |
| C18 | $\overline{\text{DBB}}$ / $\overline{\text{IRQ3}}$ |
| C19 | BADDR29 / $\overline{\text{IRQ2}}$ |
| D1 | HPE / EE1 |
| D2 | DBREQ / EE0 |
| D3 | THERM2 |
| D4 | $\overline{\text{IRQ2}}$ / DP2 / $\overline{\text{EXT\_DBG2}}$ |
| D5 | $\overline{\text{IRQ6}}$ / DP6 / $\overline{\text{DACK3}}$ |
| D6 | D8 |
| D7 | D14 |
| D8 | D19 |
| D9 | D24 |
| D10 | D29 |
| D11 | D34 / HD2 |
| D12 | D39 / HD7 |
| D13 | D43 / HD11 |
| D14 | D48 / HA0 |
| D15 | D52 / $\overline{\text{HCS1}}$ |
| D16 | D57 / HDSP |
| D17 | $\overline{\text{PWE5}}$ / $\overline{\text{PSDDQM5}}$ / $\overline{\text{PBS5}}$ |
| D18 | $\overline{\text{IRQ1}}$ / $\overline{\text{GBL}}$ |
| D19 | BADDR27 |
| E1 | BTM0 / EE4 |
| E2 | EE3 |
| E3 | EE2 |
| E4 | $V_{DDH}$ |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|--------|-------------|
| E5 | $V_{DD}$ |
| E6 | $V_{DDH}$ |
| E7 | D13 |
| E8 | $V_{DDH}$ |
| E9 | $V_{DD}$ |
| E10 | $V_{DDH}$ |
| E11 | $V_{DDH}$ |
| E12 | $V_{DD}$ |
| E13 | $V_{DDH}$ |
| E14 | D47 / HD15 |
| E15 | $V_{DDH}$ |
| E16 | D56 / $\overline{HACK}$ / $\overline{HRRQ}$ |
| E17 | PSDA10 / PGPL0 |
| E18 | MODCK1 / TC0 / BNKSEL0 |
| E19 | $\overline{PSDCAS}$ / PGPL3 |
| F1 | TDO |
| F2 | EED |
| F3 | BTM1 / EE5 |
| F4 | $V_{DD}$ |
| F5 | GND |
| F6 | $\overline{IRQ7}$ / DP7 / $\overline{DACK4}$ |
| F7 | GND |
| F8 | D18 |
| F9 | GND |
| F10 | D28 |
| F11 | GND |
| F12 | D38 / HD6 |
| F13 | GND |
| F14 | $\overline{PSDWE}$ / PGPL1 |
| F15 | GND |
| F16 | $V_{DD}$ |
| F17 | $\overline{PWE7}$ / $\overline{PSDDQM7}$ / $\overline{PBS7}$ |
| F18 | MODCK2 / TC1 / BNKSEL1 |
| F19 | $\overline{BCTL0}$ |
| G1 | PA31 / FCC1:UTOPIA8:$\overline{TXENB}$ / FCC1:MII:COL |
| G2 | TMS |
| G3 | $\overline{TRST}$ |
| G4 | TCK |
| G5 | $V_{DDH}$ |

**MSC8103 Network Digital Signal Processor, Rev. 12**

**Table 3-2.**   MSC8103 Signal Listing by Pin Designator  (Continued)

| Number | Signal Name |
|--------|-------------|
| G6 | GND |
| G7 | D12 |
| G8 | GND |
| G9 | D23 |
| G10 | GND |
| G11 | D33 / HD1 |
| G12 | GND |
| G13 | $\overline{\text{PSDVAL}}$ |
| G14 | GND |
| G15 | V$_{DDH}$ |
| G16 | V$_{DDH}$ |
| G17 | $\overline{\text{TEA}}$ |
| G18 | MODCK3 / TC2 / BNKSEL2 |
| G19 | $\overline{\text{POE}}$ / $\overline{\text{PSDRAS}}$ / PGPL2 |
| H1 | PB30 / FCC2:MII:RX_DV / SCC2:TXD / TDBM2:L1RXD |
| H2 | PD31 / SCC1:RXD / $\overline{\text{DRACK1}}$ / $\overline{\text{DONE1}}$ |
| H3 | PC31 / BRG1O / CLK1 / $\overline{\text{TGATE1}}$ |
| H4 | PB31 / FCC2:MII:TX_ER / SCC2:RXD / TDMB2:L1TXD |
| H5 | GND |
| H6 | TDI |
| H7 | GND |
| H13 | Reserved / BADDR31 / $\overline{\text{IRQ5}}$ |
| H14 | Reserved / BADDR30 / $\overline{\text{IRQ3}}$ |
| H15 | GND |
| H16 | V$_{DD}$ |
| H17 | $\overline{\text{BR}}$ |
| H18 | ALE |
| H19 | $\overline{\text{PWE4}}$ / $\overline{\text{PSDDQM4}}$ / $\overline{\text{PBS4}}$ |
| J1 | PA29 / FCC1:UTOPIA8:TXSOC / FCC1:MII:TX_ER |
| J2 | PD30 / SCC1:TXD / DMA:$\overline{\text{DRACK2}}$/$\overline{\text{DONE2}}$ |
| J3 | PC30 / EXT1 / BRG2O / CLK2 / $\overline{\text{TOUT1}}$ |
| J4 | V$_{DD}$ |
| J5 | GND |
| J6 | GND |
| J7 | PA30 / FCC1:UTOPIA8:TXCLAV / FCC1:UTOPIA8:TXCLAV0 / FCC1:MII:CRS / FCC1:HDLC and transparent:$\overline{\text{RTS}}$ |
| J13 | $\overline{\text{TA}}$ |
| J14 | GND |
| J15 | V$_{DDH}$ |

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**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|--------|-------------|
| J16 | $V_{DDH}$ |
| J17 | PSDAMUX / PGPL5 |
| J18 | $\overline{\text{PGTA}}$ / PUPMWAIT / $\overline{\text{PPBS}}$ / PGPL4 |
| J19 | $\overline{\text{PWE3}}$ / $\overline{\text{PSDDQM3}}$ / $\overline{\text{PBS3}}$ |
| K1 | PA28 / FCC1:UTOPIA8:$\overline{\text{RXENB}}$ / FCC1:MII:TX_EN |
| K2 | PD29 / FCC1:UTOPIA8:RXADDR3 / FCC1:UTOPIA8:RXCLAV2 / SCC1:$\overline{\text{RTS}}$/TENA |
| K3 | PC29 / SCC1:$\overline{\text{CTS}}$ / SCC1:CLSN / BRG3O / CLK3 / TIN2 |
| K4 | PB29 / FCC2:MII:TX_EN / TDMB2:L1RSYNC |
| K5 | $V_{DDH}$ |
| K6 | GND |
| K7 | GND |
| K13 | GND |
| K14 | $\overline{\text{PWE2}}$ / $\overline{\text{PSDDQM2}}$ / $\overline{\text{PBS2}}$ |
| K15 | GND |
| K16 | $V_{DDH}$ |
| K17 | $\overline{\text{PWE1}}$ / $\overline{\text{PSDDQM1}}$ / $\overline{\text{PBS1}}$ |
| K18 | $\overline{\text{PWE0}}$ / $\overline{\text{PSDDQM0}}$ / $\overline{\text{PBS0}}$ |
| K19 | $\overline{\text{CS2}}$ |
| L1 | PA27 / FCC1:UTOPIA8:RXSOC / FCC1:MII:RX_DV |
| L2 | PB28 / FCC2:RX_ER / FCC2:HDLC:$\overline{\text{RTS}}$ / SCC2:$\overline{\text{RTS}}$/TENA / TDMB2:L1TSYNC |
| L3 | PC28 / SCC2:$\overline{\text{CTS}}$/CLSN / BRG4O / CLK4 / TIN1/$\overline{\text{TOUT2}}$ |
| L4 | $V_{DD}$ |
| L5 | GND |
| L6 | GND |
| L7 | PC27 / CLK5 / BRG5O / $\overline{\text{TGATE2}}$ |
| L13 | $\overline{\text{CS6}}$ |
| L14 | GND |
| L15 | GND |
| L16 | $V_{DD}$ |
| L17 | $\overline{\text{CS1}}$ |
| L18 | $\overline{\text{CS3}}$ |
| L19 | $\overline{\text{BCTL1}}$ |
| M1 | PB27 / FCC2:MII:COL / TDMC2:L1TXD |
| M2 | PC26 / TMCLK / BRG6O / CLK6 / $\overline{\text{TOUT3}}$ |
| M3 | PB26 / FCC2:MII:CRS / TDMC2:L1RXD |
| M4 | $V_{DDH}$ |
| M5 | GND |
| M6 | PA26 / FCC1:UTOPIA8:RXCLAV / FCC1:UTOPIA8:RXCLAV0 / FCC1:MII:RX_ER |

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**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|--------|-------------|
| M7 | PA16 / FCC1:UTOPIA8:RXD6 / FCC1:MII and HDLC nibble:RXD1 |
| M13 | A21 |
| M14 | A26 |
| M15 | GND |
| M16 | $\overline{CS0}$ |
| M17 | $\overline{CS5}$ |
| M18 | $\overline{CS7}$ |
| M19 | $\overline{CS4}$ |
| N1 | PC25 / DMA:$\overline{DACK2}$ / BRG7O / CLK7 / TIN4 |
| N2 | PA25 / FCC1:UTOPIA8:TXD0 / SDMA:MSNUM0 |
| N3 | PB25 / FCC2:MII and HDLC nibble:TXD3 / TDMA1:nibble:L1TXD3 / TDMC2:L1TSYNC |
| N4 | $V_{DD}$ |
| N5 | PC23 / EXT2 / DMA:$\overline{DACK1}$ / CLK9 |
| N6 | GND |
| N7 | PD17 / FCC1:UTOPIA8:RXPRTY / SPI:SPIMOSI / BRG2O |
| N8 | CLKIN |
| N9 | GND |
| N10 | PC6 / FCC1:UTOPIA8:RXADDR2 / FCC1:UTOPIA8:RXADDR2/RXCLAV1 / FCC1:$\overline{CD}$ / SI2:LIST2 |
| N11 | TSIZ3 |
| N12 | TT1 |
| N13 | TT0 |
| N14 | A1 |
| N15 | $V_{DDH}$ |
| N16 | $V_{DDH}$ |
| N17 | A28 |
| N18 | A30 |
| N19 | A31 |
| P1 | PC24 / DMA:DREQ2 / BRG8O / CLK8 / TIN3$\overline{TOUT4}$ |
| P2 | PA24 / FCC1:UTOPIA8:TXD1 / SDMA:MSNUM1 |
| P3 | PB24 / FCC2:MII and HDLC nibble:TXD2 / TDMA1:nibble:L1RXD3 / TDMC2:L1RSYNC |
| P4 | PA23 / FCC1:UTOPIA8:TXD2 |
| P5 | PB20 / FCC2:MII and HDLC nibble:RXD1 / TDMA1:nibble:L1TXD1 / TDMD2:L1RSYNC |
| P6 | GND |
| P7 | GND |
| P8 | DLLIN |
| P9 | GND |

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**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|--------|-------------|
| P10 | PC4 / FCC2:$\overline{\text{CD}}$ / SMC1:SMRXD / SI2:LIST4 |
| P11 | GND |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P15 | GND |
| P16 | V$_{DD}$ |
| P17 | A23 |
| P18 | A27 |
| P19 | A29 |
| R1 | PC22 / SI1:LIST1 / DREQ1 / CLK10 |
| R2 | SPARE1 |
| R3 | PA22 / FCC1:UTOPIA8:TXD3 |
| R4 | PB18 / FCC2:MII and HDLC nibble:RXD3 / I$^2$C:SCL |
| R5 | PA19 / FCC1:UTOPIA8:TXD6 / FCC1:MII and HDLC nibble:TXD1 |
| R6 | V$_{DDH}$ |
| R7 | V$_{DDH}$ |
| R8 | V$_{DD}$ |
| R9 | V$_{DDH}$ |
| R10 | V$_{DDH}$ |
| R11 | V$_{DD}$ |
| R12 | V$_{DDH}$ |
| R13 | V$_{DD}$ |
| R14 | V$_{DDH}$ |
| R15 | V$_{DDH}$ |
| R16 | A15 |
| R17 | A19 |
| R18 | A24 |
| R19 | A25 |
| T1 | PB21 / FCC2:MII and HDLC nibble:RXD0 / FCC2:transparent and HDLC serial:RXD /TDMA1:nibble:L1TXD2 / TDMD2:L1TSYNC |
| T2 | PB22 / FCC2:MII and HDLC nibble TXD0 / FCC2:transparent and HDLC serial TXD /TDMA1:nibble L1RXD1 / TDMD2:L1RXD |
| T3 | PA20 / FCC1:UTOPIA8 TXD5 / FCC1:MII and HDLC nibble TXD2 |
| T4 | PA17 / FCC1:UTOPIA8 RXD7 / FCC1:MII and HDLC nibble RXD0 / FCC1:transparent and HDLC serial RXD |
| T5 | PC13 / FCC1:UTOPIA8:TXADDR1 / SCC2:$\overline{\text{CTS}}$/CLSN / SI1:LIST4 |
| T6 | PC14 / FCC1:UTOPIA8:RXADDR0 / SCC1:$\overline{\text{CD}}$/RENA / SI1:LIST2 |
| T7 | V$_{CCSYN1}$ |

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**Table 3-2.**    MSC8103 Signal Listing by Pin Designator  (Continued)

| Number | Signal Name |
|--------|-------------|
| T8 | CLKOUT |
| T9 | PA12 / FCC1:UTOPIA8:RXD2 / SDMA:MSNUM3 |
| T10 | PC7 / FCC1:UTOPIA8:TXADDR2 / FCC1:UTOPIA8:TXADDR2/TXCLAV1 / FCC1:$\overline{\text{CTS}}$ / SI1:LIST1 |
| T11 | PA6 / TDMA1:L1RSYNC |
| T12 | $\overline{\text{AACK}}$ |
| T13 | $\overline{\text{TS}}$ |
| T14 | A3 |
| T15 | V$_{\text{DDH}}$ |
| T16 | A12 |
| T17 | A16 |
| T18 | A20 |
| T19 | A22 |
| U1 | PA21 / FCC1:TXD4 / FCC1:MII and HDLC nibble TXD3 |
| U2 | PB19 / FCC2:MII and HDLC nibble RXD2 / I$^2$C:SDA |
| U3 | PD18 / FCC1:UTOPIA8:RXADDR4 / FCC1:UTOPIA8:RXCLAV3 / SPI:SPICLK |
| U4 | PD16 / FCC1:UTOPIA8:TXPRTY / SPI:SPIMISO |
| U5 | $\overline{\text{NMI}}$ |
| U6 | $\overline{\text{RSTCONF}}$ |
| U7 | GND$_{\text{SYN1}}$ |
| U8 | PA13 / FCC1:UTOPIA8:RXD3 / SDMA:MSNUM2 |
| U9 | PA10 / FCC1:UTOPIA8:RXD0 / SDMA:MSNUM5 |
| U10 | PA8 / SMC2:SMRXD / TDMA1:serial L1RXD / TDMA1:nibble L1RXD0 |
| U11 | SPARE5 |
| U12 | $\overline{\text{ARTRY}}$ |
| U13 | $\overline{\text{TBST}}$ |
| U14 | TT2 |
| U15 | A4 |
| U16 | A8 |
| U17 | A11 |
| U18 | A17 |
| U19 | A18 |
| V1 | PB23 / FCC2:MII and HDLC nibble:TXD1 / TDMA1:nibble:L1RXD2 / TDMD2:L1TXD |
| V2 | PD19 / FCC1:UTOPIA8:TXADDR4 / FCC1:UTOPIA:TXCLAV3 / SPI:$\overline{\text{SPISEL}}$ / BRG1O |
| V3 | PC15 / FCC1:UTOPIA8:TXADDR0 / SCC1:$\overline{\text{CTS}}$/CLSN / SMC2:SMTXD |
| V4 | PC12 / FCC1:UTOPIA8:RXADDR1 / SCC2:$\overline{\text{CD}}$/RENA / SI1:LIST3 |
| V5 | $\overline{\text{NMI\_OUT}}$ |
| V6 | $\overline{\text{HRESET}}$ |

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**Table 3-2.**    MSC8103 Signal Listing by Pin Designator  (Continued)

| Number | Signal Name |
|--------|-------------|
| V7 | GND$_{SYN}$ |
| V8 | PA11 / FCC1:UTOPIA8:RXD1 / SDMA:MSNUM4 |
| V9 | PD7 / FCC1:UTOPIA8:TXADDR3 / FCC1:UTOPIA8:TXCLAV2 / SMC1:$\overline{\text{SMSYN}}$ |
| V10 | PA7 / SMC2:$\overline{\text{SMSYN}}$ / TDMA1:L1TSYNC |
| V11 | $\overline{\text{ABB}}$ / $\overline{\text{IRQ2}}$ |
| V12 | $\overline{\text{BG}}$ |
| V13 | TSIZ0 |
| V14 | TT3 |
| V15 | A2 |
| V16 | A6 |
| V17 | A9 |
| V18 | A13 |
| V19 | A14 |
| W2 | PA18 / FCC1:UTOPIA8:TXD7 / FCC1:MII and HDLC nibble:TXD0 / FCC1:transparent and HDLC serial:TXD |
| W3 | PA15 / FCC1:UTOPIA8:RXD5 / FCC1:MII and HDLC nibble:RXD2 |
| W4 | $\overline{\text{SRESET}}$ |
| W5 | $\overline{\text{PORESET}}$ |
| W6 | TEST |
| W7 | V$_{CCSYN}$ |
| W8 | PA14 / FCC1:UTOPIA8 RXD4 / FCC1:MII and HDLC nibble:RXD3 |
| W9 | PA9 / SMC2:SMTXD / TDMA1:serial:L1TXD /TDMA1:nibble:L1TXD0 |
| W10 | PC5 / FCC2:$\overline{\text{CTS}}$ / SMC1:SMTXD / SI2:LIST3 |
| W11 | $\overline{\text{IRQ7}}$ / $\overline{\text{INT\_OUT}}$ |
| W12 | TSIZ2 |
| W13 | TSIZ1 |
| W14 | TT4 |
| W15 | A0 |
| W16 | A5 |
| W17 | A7 |
| W18 | A10 |

# 3.2 Lidded FC-PBGA Package Mechanical Drawing



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.

2. Dimensions in millimeters.

⚠ Maximum solder ball diameter measured parallel to Datum A.

⚠ Primary Datum A and the seating plane are defined by the spherical crowns of the solder balls.
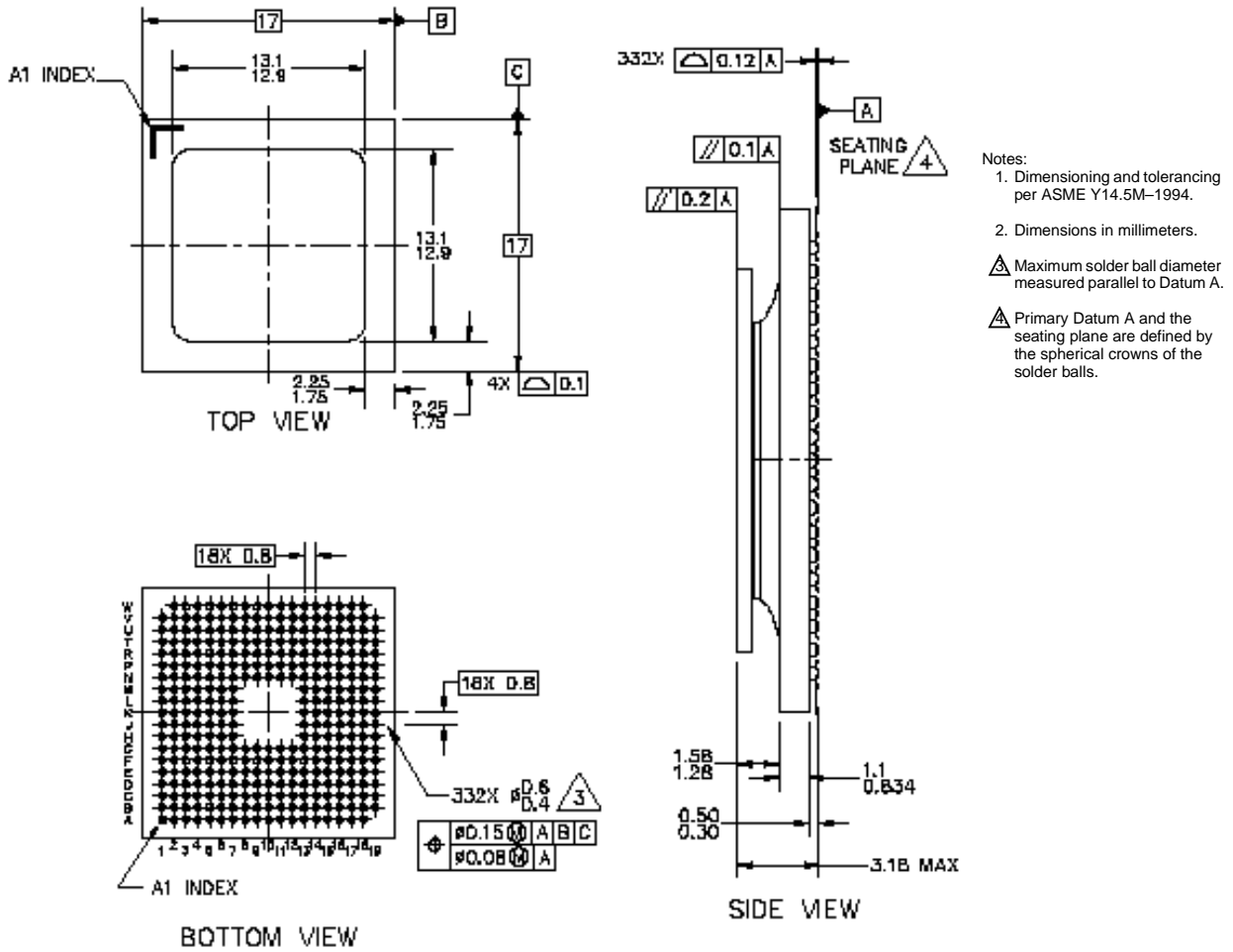
**CASE 1473-01**

**Figure 3-3.** Case 1473-01 Mechanical Information, 332-pin Lidded FC-PBGA Package

# Design Considerations 4

This chapter includes design and layout guidelines for manufacturing boards using the MSC8103.

## 4.1  Thermal Design Considerations

The average chip-junction temperature, $T_J$, in °C can be obtained from the following:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

**Equation 1**

where

$T_A$ = ambient temperature °C

$\theta_{JA}$ = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$ in W

$P_{INT} = I_{DD} \times V_{DD}$ in W—chip internal power

$P_{I/O}$ = power dissipation on output pins in W—user determined

The user should set $T_A$ and $P_D$ such that $T_J$ does not exceed the maximum operating conditions. In case $T_J$ is too high, the user should either lower the ambient temperature or the power dissipation of the chip.

## 4.2  Electrical Design Considerations

The input voltage must not exceed the I/O supply $V_{DDH}$ by more than 2.5 V at any time, including during power-on reset. In turn, $V_{DDH}$ can exceed $V_{DD}/V_{CCSYN}$ by more than 3.3 V during power-on reset, but for no more than 100 ms. $V_{DDH}$ should not exceed $V_{DD}/V_{CCSYN}$ by more than 2.1 V during normal operation. $V_{DD}/V_{CCSYN}$ must not exceed $V_{DDH}$ by more than 0.4 V at any time, including during power-on reset. Therefore the recommendation is to use "bootstrap" diodes between the power rails, as shown in **Figure 4-1**.
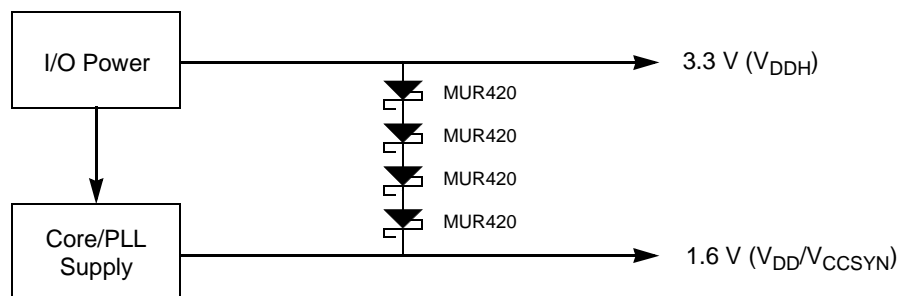


**Figure 4-1.**  Bootstrap Diodes for Power-Up Sequencing

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Select the bootstrap diodes such that a nominal $V_{DD}/V_{CCSYN}$ is sourced from the $V_{DDH}$ power supply until the $V_{DD}/V_{CCSYN}$ power supply becomes active. In **Figure 4-1**, four MUR420 Schottky barrier diodes are connected in series; each has a forward voltage ($V_F$) of 0.6 V at high currents, so these diodes provide a 2.4 V drop, maintaining 0.9 V on the 1.6 V power line. Once the core/PLL power supply stabilizes at 1.6 V, the bootstrap diodes will be reverse biased with negligible leakage current. The $V_F$ should be effective at the current levels required by the processor. Do not use diodes with a nominal $V_F$ that drops too low at high current.

# 4.3  Power Considerations

The internal power dissipation consists of three components:

$$P_{INT} = P_{CORE} + P_{SIU} + P_{CPM}$$

Power dissipation depends on the operating frequency of the different portions of the chip. **Table 2-5** provides typical power values at the specified operating frequencies. To determine the typical power dissipation for a given set of frequencies, use the following equations:

$$P_{CORE}\ (f) = ((P_{CORE} - P_{LCO})/f_{CORE}) \times f_{COREA} + P_{LCO}$$
$$P_{CPM}\ (f) = ((P_{CPM} - P_{LCP})/f_{CPM}) \times f_{CPMA} + P_{LCP}$$
$$P_{SIU}\ (f) = ((P_{SIU} - P_{LSI})/f_{SIU}) \times f_{SIUA} + P_{LSI}$$

Where:

- $f_{CORE}$ is the core frequency, $f_{SIU}$ is the SIU frequency, and $f_{CPM}$ is the CPM frequency specified in **Table 2-5** in MHz

- $f_{COREA}$ is the actual core frequency, $F_{SIUA}$ is the actual SIU frequency, and $F_{CPMA}$ is the actual CPM frequency in MHz

- $P_{LCO}$, $P_{LSI}$, and $P_{LCP}$ are the leakage power values specified in **Table 2-5**

- All power numbers are in mW

- Power consumption is assumed to be linear with frequency. The first part of each equation computes a mw/MHz value that is then scaled based on the actual frequency used.

To determine a total power dissipation in a specific application, you must add the power values derived from the above set of equations to the value derived for I/O power consumption using the following equation for each output pin:

$$\textbf{P} = \textbf{C} \times \textbf{V}_{\textbf{DDH}}{}^{\textbf{2}} \times \textbf{f} \times \textbf{10}^{\textbf{–3}} \qquad\qquad \textbf{Equation 2}$$

Where: P = power in mW, C = load capacitance in pF, f = output switching frequency in MHz.

For an application in which external data memory is used in a 32-bit single bus mode and no other outputs are active, the core runs at 200 MHz, the CPM runs at 100 MHz and the SIU runs at 50 MHz, power dissipation is calculated as follows:

*Assumptions:*

- External data memory is accessed every second cycle with 10% of address pins switching.

- External data memory writes occurs once every eight cycles with 50% of data pins switching.

- Each address and data pin has a 30 pF total load at the pin.

- The application operates at $V_{DDH}$ = 3.3 V.

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Since the address pins switch once at every second cycle, the address pins frequency is a quarter of the bus frequency (that is, 25 MHz).

For the same reason the data pins frequency is 3.125 MHz.

**Table 4-1.** Power Dissipation

| Pins | Number of Pins Switching | $\times$ C | $\times$ $V_{DDH}^2$ | $\times f \times 10^{-3}$ | Power in mW |
|---|---|---|---|---|---|
| Address <br> Data, $\overline{HRD}$, $\overline{HRW}$ <br> CLKOUT | 4 <br> 34 <br> 1 | $\times 30$ <br> $\times 30$ <br> $\times 30$ | $\times 3.3^2$ <br> $\times 3.3^2$ <br> $\times 3.3^2$ | $\times 12.5 \times 10^{-3}$ <br> $\times 3.125 \times 10^{-3}$ <br> $\times 50 \times 10^{-3}$ | 16.25 <br> 34.75 <br> 16 |
| Total $P_{I/O}$ | | | | | 67 |

Calculating internal power (from **Table 2-5** values):

$P_{CORE} (200) = ((P_{CORE} - P_{LCO})/300) \times 200 + P_{LCO} = ((450 - 3) / 300 \times 200 + 3 = 301$

$P_{CPM} (100) = ((P_{CPM} - P_{LCP}) / 200) \times 100 + P_{LCP} = ((320 - 6) / 200) \times 100 + 6 = 163$

$P_{SIU} (50) = ((P_{SIU} - P_{LSI}) / 100) \times 50 + P_{LSI} = ((80 - 2) / 100) \times 50 + 2 = 41$

$P_{INT} = P_{CORE}(200) + P_{CPM}(100) + P_{SIU}(50) = 301 + 163 + 41 = 505$

$P_D = P_{INT} + P_{I/O} = 505 + 67 = 572$

Maximum allowed ambient temperature is:

$T_A = T_J - (PD \times \theta_{JA})$

# 4.4  Layout Practices

Each $V_{CC}$ and $V_{DD}$ pin on the MSC8103 should be provided with a low-impedance path to the board's power supply. Similarly, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$, $V_{DD}$, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MSC8103 have fast rise and fall times. Printed circuit board (PCB) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PCB trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$, $V_{DD}$, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

There are 2 pairs of PLL supply pins: $V_{CCSYN}$-$GND_{SYN}$ and $V_{CCSYN1}$-$GND_{SYN1}$. Each pair supplies one PLL. To ensure internal clock stability, filter the power to the $V_{CCSYN}$ and $V_{CCSYN1}$ inputs with a circuit similar to the one in **Figure 4-2**. To filter as much noise as possible, place the circuit as close as possible to $V_{CCSYN}$ and $V_{CCSYN1}$. The 0.01-μF capacitor should be closest to $V_{CCSYN}$ and $V_{CCSYN1}$, followed by the 10-μF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to $V_{DD}$. These traces should be kept short and direct.

GND$_{SYN}$ and GND$_{SYN1}$ should be provided with an extremely low impedance path to ground and should be bypassed to V$_{CCSYN}$ and V$_{CCSYN1}$, respectively, by a 0.01-µF capacitor located as close as possible to the chip package. The user should also bypass GND$_{SYN}$ and GND$_{SYN1}$ to V$_{CCSYN}$ and V$_{CCSYN1}$ with a 0.01-µF capacitor as closely as possible to the chip package
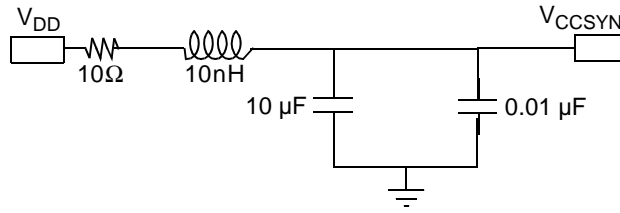


**Figure 4-2.** VCCSYN and VCCSYN1 Bypass

# Ordering Information

For product availability, consult a Freescale Semiconductor sales office or authorized distributor.

| Part | Supply Voltage | Package Type | Pin Count | Mask Set | Sphere Type | Core Frequency (MHz) | Order Number |
|---|---|---|---|---|---|---|---|
| MSC8103 | 1.6 V core 3.3 V I/O | Lidded Flip Chip Plastic Ball Grid Array (FC-PBGA) | 332 | 2K87M | Pb-bearing | 275 | MSC8103M1100F |
| | | | | | Pb-free | 275 | MSC8103VT1100F |
| | | | | | Pb-bearing | 300 | MSC8103M1200F |
| | | | | | Pb-free | 300 | MSC8103VT1200F |

MSC8103
Rev. 12
8/2005

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